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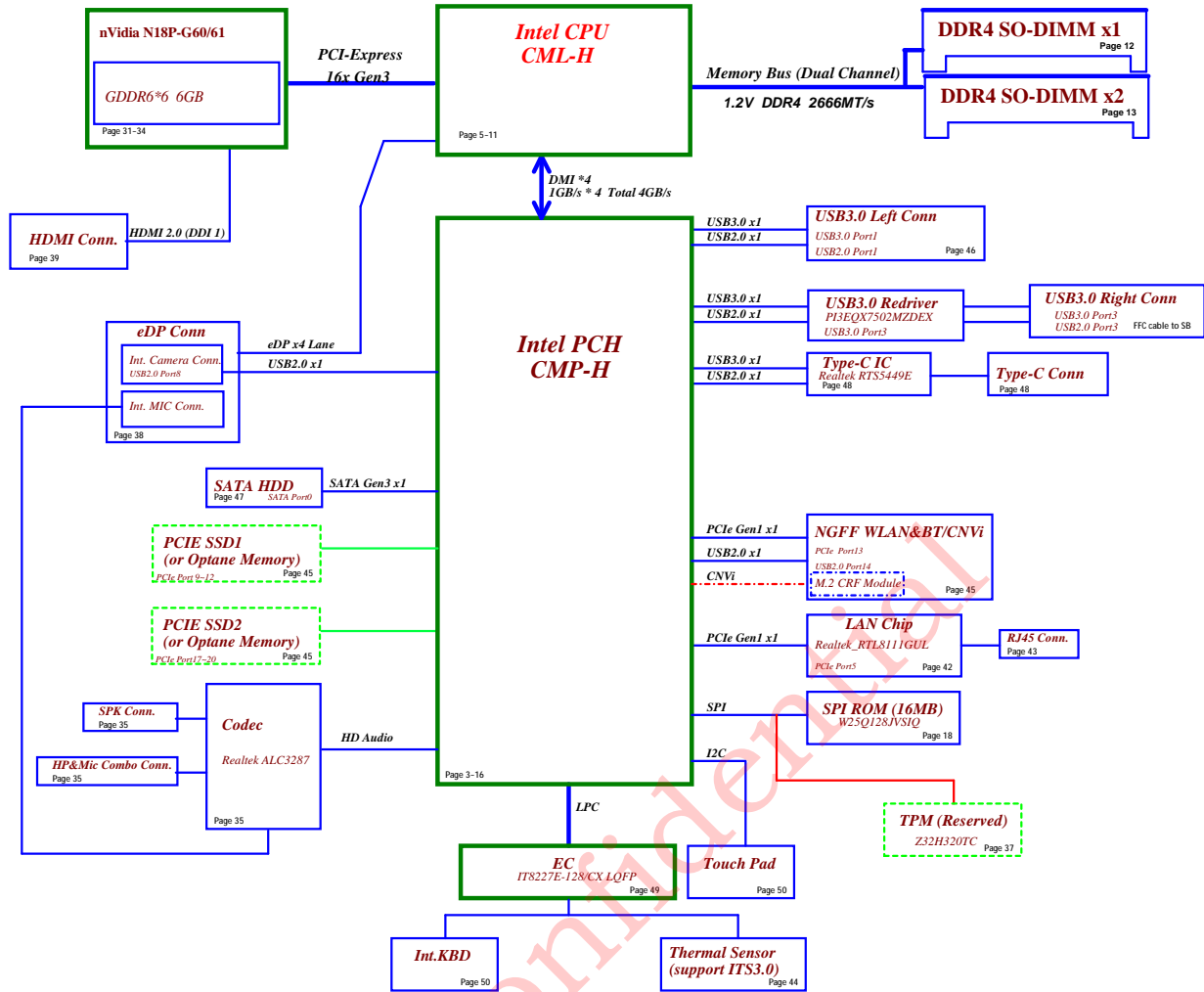
L350-IMH +N18P-G61/62 MB Schematics Document

Comet Lake-H with DDR4 + Nvidia N18P-G61/62

2019-06-10

REV:0.1

Security Classification	LC Future Center Secret Data			Title	Cover Page	
Issued Date	2015/08/20	Deciphered Date	2018/09/20	Size	Document Number	Rev
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				Date	Sunday, October 28, 2019	Sheet 1 of 75



Security Classification	LC Future Center Secret Data		Title	Block Diagram	
Issued Date	2015/08/20	Deciphered Date	2018/09/20	Size	Document Number
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			Issue	2	1

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GZ +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALN	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIE	1-4 DGPU
	K4 PCIE
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9-12 Optane Memory
	K4 PCIE
SATA	0 HDD
	1A ODD
	1B used as PCIE
	2 used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
17@	For 17" part
15or17@	For 15" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
TS@	For touch screen part
TS_NS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
EX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAM rank part
DUALRANK@	For Dual VRAM rank part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT9586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WIMAX
EC_SMB_CK1	IT9586E	V	V	X	V	X	X	X	X	X	X
EC_SMB_DA1	+3VL_EC				+3VL_EC						
EC_SMB_CK2	IT9586E	X	X	V	V	X	V	X	X	V	X
EC_SMB_DA2	+3VS			+3VG_AON	+3VS		+3VALW_PCH				
EC_SMB_CK3	IT9586E	X	X	X	V	X	X	V	X	X	X
EC_SMB_DA3	+3VL_EC				+3VL_EC						
PCH_SMB_CLK	PCH	X	X	X	X	X	V	X	V	X	V
PCH_SMB_DATA	+3VALW_PCH						+3VALW_PCH		+3VS		+3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100b
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DOR4 SODIMM	need to update
Wlan	Reserved

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Rev	01	Document Number	GY530
Issue	Sunday, October 25, 2016	Issue	3 of 75

[25] PCIe_CRX_GTX_N0_15] [25]
[25] PCIe_CRX_GTX_P0_15] [25]
[25] PCIe_CTX_C_GRX_N0_15] [25]
[25] PCIe_CTX_C_GRX_P0_15] [25]

VCCIO

CAD Note:
Place R_comp inside CPU cavity
Trace width=12 mils. Spacing=15mil
Max length= 400 mils.

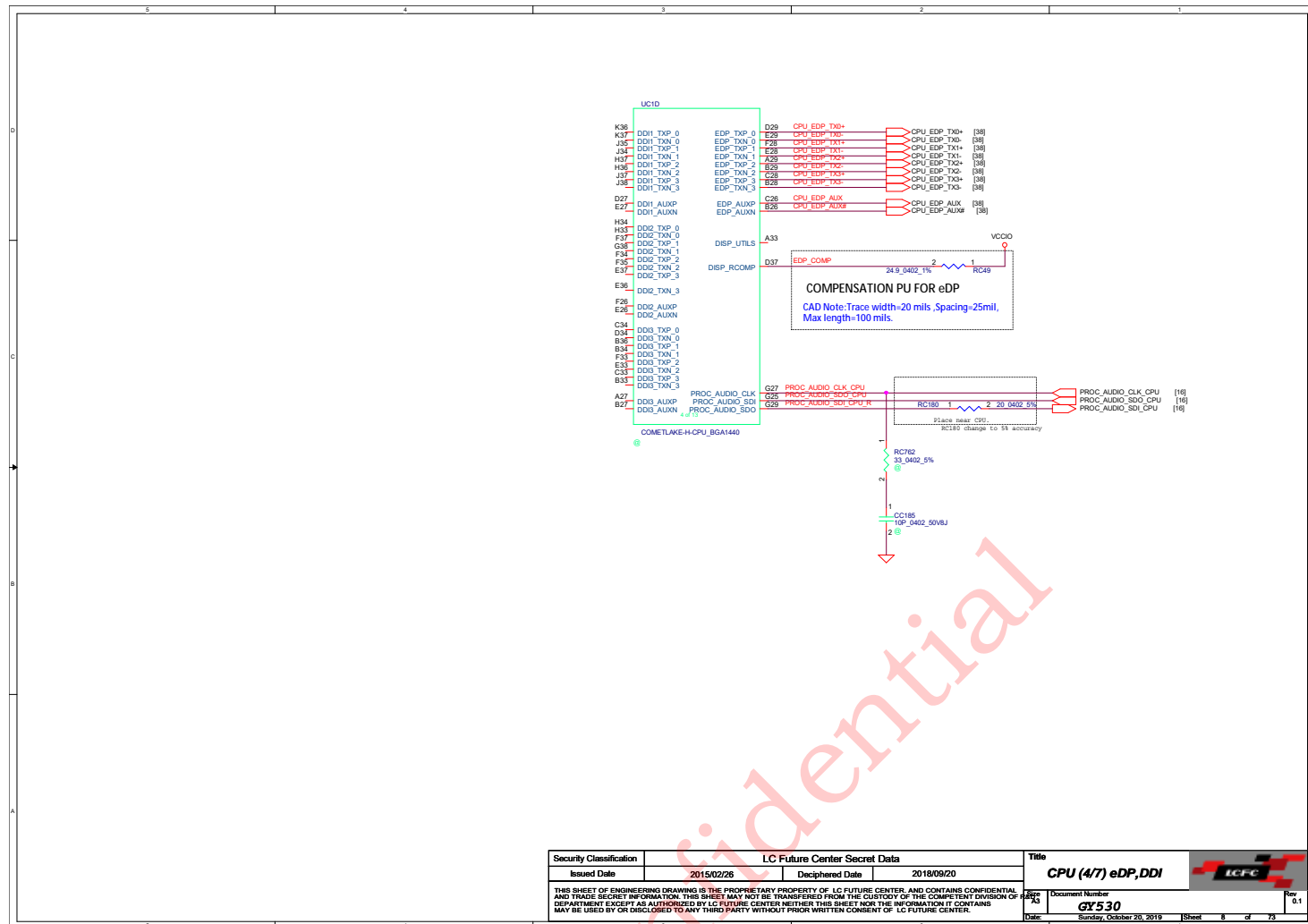
RC1 2 1 24.9 9402 1%

UCIC									
PCIe_CRX_GTX_P15	E25	REG_RXP_0	PEG_TXP_0	B25	PCIe_CTX_GRX_P15	OPTB	CC32	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N15	E25	REG_RXP_0	PEG_TXP_0	A25	PCIe_CTX_GRX_N15	OPTB	CC16	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P14	E24	REG_RXP_1	PEG_TXP_1	B24	PCIe_CTX_GRX_P14	OPTB	CC31	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N14	E24	REG_RXP_1	PEG_TXP_1	A24	PCIe_CTX_GRX_N14	OPTB	CC15	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P13	E23	REG_RXP_2	PEG_TXP_2	B23	PCIe_CTX_GRX_P13	OPTB	CC30	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N13	E23	REG_RXP_2	PEG_TXP_2	A23	PCIe_CTX_GRX_N13	OPTB	CC14	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P12	E22	REG_RXP_3	PEG_TXP_3	B22	PCIe_CTX_GRX_P12	OPTB	CC29	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N12	E22	REG_RXP_3	PEG_TXP_3	A22	PCIe_CTX_GRX_N12	OPTB	CC13	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P11	E21	REG_RXP_4	PEG_TXP_4	B21	PCIe_CTX_GRX_P11	OPTB	CC28	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N11	E21	REG_RXP_4	PEG_TXP_4	A21	PCIe_CTX_GRX_N11	OPTB	CC12	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P10	E20	REG_RXP_5	PEG_TXP_5	B20	PCIe_CTX_GRX_P10	OPTB	CC27	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N10	E20	REG_RXP_5	PEG_TXP_5	A20	PCIe_CTX_GRX_N10	OPTB	CC11	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P9	E19	REG_RXP_6	PEG_TXP_6	B19	PCIe_CTX_GRX_P9	OPTB	CC26	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N9	E19	REG_RXP_6	PEG_TXP_6	A19	PCIe_CTX_GRX_N9	OPTB	CC10	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P8	E18	REG_RXP_7	PEG_TXP_7	B18	PCIe_CTX_GRX_P8	OPTB	CC25	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N8	E18	REG_RXP_7	PEG_TXP_7	A18	PCIe_CTX_GRX_N8	OPTB	CC9	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P7	E17	REG_RXP_8	PEG_TXP_8	A17	PCIe_CTX_GRX_P7	OPTB	CC24	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N7	E17	REG_RXP_8	PEG_TXP_8	B17	PCIe_CTX_GRX_N7	OPTB	CC8	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P6	E16	REG_RXP_9	PEG_TXP_9	C16	PCIe_CTX_GRX_P6	OPTB	CC23	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N6	E16	REG_RXP_9	PEG_TXP_9	B16	PCIe_CTX_GRX_N6	OPTB	CC7	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P5	E15	REG_RXP_10	PEG_TXP_10	A15	PCIe_CTX_GRX_P5	OPTB	CC22	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N5	E15	REG_RXP_10	PEG_TXP_10	B15	PCIe_CTX_GRX_N5	OPTB	CC6	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P4	E14	REG_RXP_11	PEG_TXP_11	C14	PCIe_CTX_GRX_P4	OPTB	CC21	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N4	E14	REG_RXP_11	PEG_TXP_11	B14	PCIe_CTX_GRX_N4	OPTB	CC5	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P3	E13	REG_RXP_12	PEG_TXP_12	A13	PCIe_CTX_GRX_P3	OPTB	CC20	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N3	E13	REG_RXP_12	PEG_TXP_12	B13	PCIe_CTX_GRX_N3	OPTB	CC4	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P2	E12	REG_RXP_13	PEG_TXP_13	C12	PCIe_CTX_GRX_P2	OPTB	CC19	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N2	E12	REG_RXP_13	PEG_TXP_13	B12	PCIe_CTX_GRX_N2	OPTB	CC3	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P1	E11	REG_RXP_14	PEG_TXP_14	A11	PCIe_CTX_GRX_P1	OPTB	CC18	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N1	E11	REG_RXP_14	PEG_TXP_14	B11	PCIe_CTX_GRX_N1	OPTB	CC2	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_P0	E10	REG_RXP_15	PEG_TXP_15	C10	PCIe_CTX_GRX_P0	OPTB	CC17	1	2 0.22U 0201 6.3V6-K
PCIe_CRX_GTX_N0	E10	REG_RXP_15	PEG_TXP_15	B10	PCIe_CTX_GRX_N0	OPTB	CC1	1	2 0.22U 0201 6.3V6-K
DM1_CRX_PTX_P0	D8	DM1_RXP_0	DM1_TXN_0	B8	DM1_CTX_PRX_P0				DM1_CTX_PRX_P0 [19]
DM1_CRX_PTX_N0	D8	DM1_RXP_0	DM1_TXN_0	A8	DM1_CTX_PRX_N0				DM1_CTX_PRX_N0 [19]
DM1_CRX_PTX_P1	D6	DM1_RXP_1	DM1_TXN_1	C6	DM1_CTX_PRX_P1				DM1_CTX_PRX_P1 [19]
DM1_CRX_PTX_N1	D6	DM1_RXP_1	DM1_TXN_1	B6	DM1_CTX_PRX_N1				DM1_CTX_PRX_N1 [19]
DM1_CRX_PTX_P2	D5	DM1_RXP_2	DM1_TXN_2	B5	DM1_CTX_PRX_P2				DM1_CTX_PRX_P2 [19]
DM1_CRX_PTX_N2	D5	DM1_RXP_2	DM1_TXN_2	A5	DM1_CTX_PRX_N2				DM1_CTX_PRX_N2 [19]
DM1_CRX_PTX_P3	D4	DM1_RXP_3	DM1_TXN_3	C4	DM1_CTX_PRX_P3				DM1_CTX_PRX_P3 [19]
DM1_CRX_PTX_N3	D4	DM1_RXP_3	DM1_TXN_3	B4	DM1_CTX_PRX_N3				DM1_CTX_PRX_N3 [19]

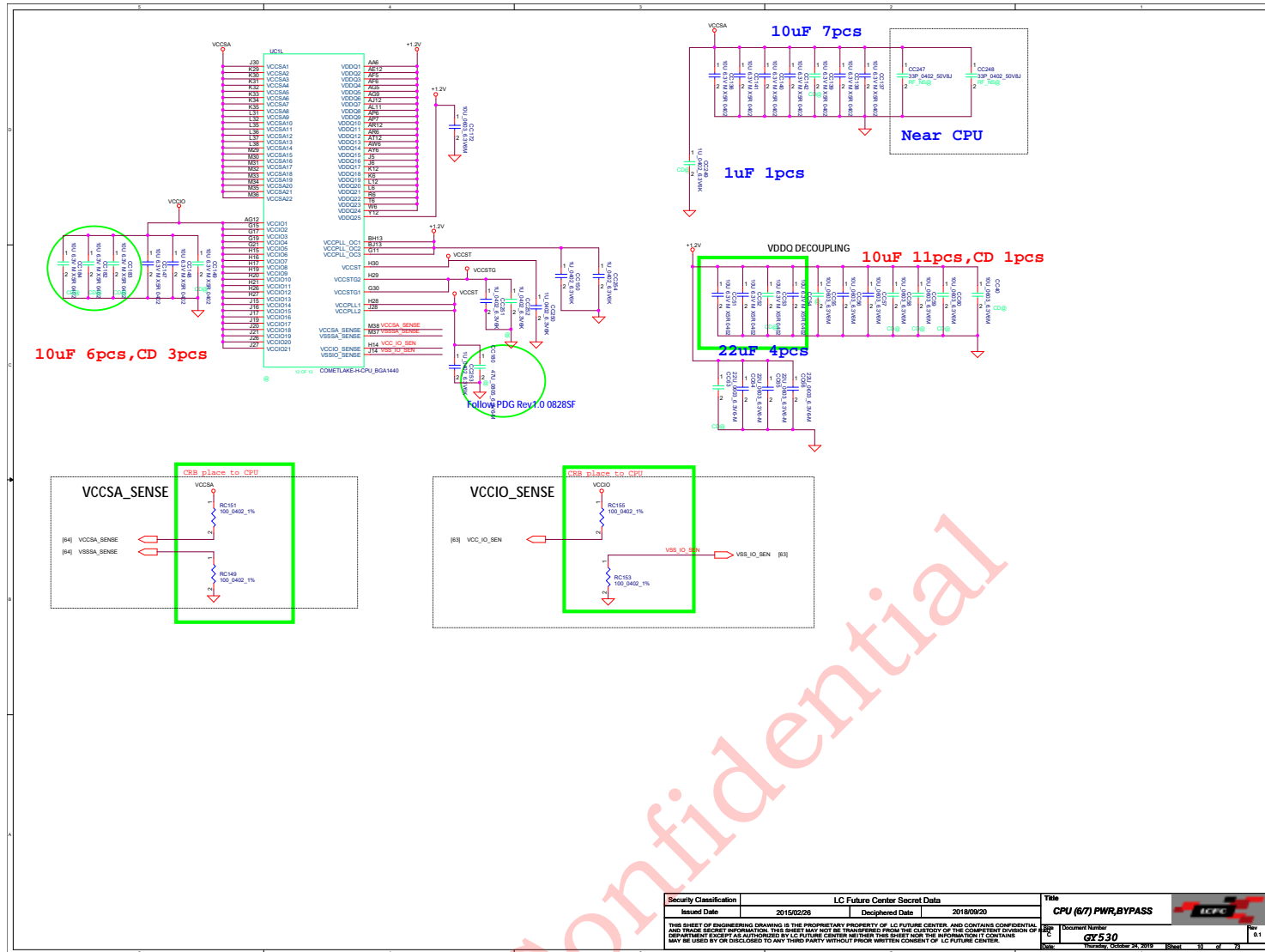
COMETLAKE-H CPU_BGA1440

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Title		LCFC	
CPU (1/7) DM1,PEG			
Size	Document Number		
Custom	QY530		
Date	Sunday, October 26, 2019	Sheet	5 of 75



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/26	Deciphered Date	2018/09/20	CPU (47) eDP, DDI	
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				Date	GY530
				Sheet	8 of 73



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Issued Date	2015/02/26	Deciphered Date	2018/09/20	CPU (G7) PWR,BYPASS	
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Doc No.		GY 530		Rev. 0.1	
Date		2015/02/26		Rev. 1	
Rev.		1		Rev. 1	

LCIF		
A10	VSS 100	AK4
A11	VSS 101	AK4
A12	VSS 102	AK4
A13	VSS 103	AK4
A14	VSS 104	AK4
A15	VSS 105	AK4
A16	VSS 106	AK4
A17	VSS 107	AK4
A18	VSS 108	AK4
A19	VSS 109	AK4
A20	VSS 110	AK4
A21	VSS 111	AK4
A22	VSS 112	AK4
A23	VSS 113	AK4
A24	VSS 114	AK4
A25	VSS 115	AK4
A26	VSS 116	AK4
A27	VSS 117	AK4
A28	VSS 118	AK4
A29	VSS 119	AK4
A30	VSS 120	AK4
A31	VSS 121	AK4
A32	VSS 122	AK4
A33	VSS 123	AK4
A34	VSS 124	AK4
A35	VSS 125	AK4
A36	VSS 126	AK4
A37	VSS 127	AK4
A38	VSS 128	AK4
A39	VSS 129	AK4
A40	VSS 130	AK4
A41	VSS 131	AK4
A42	VSS 132	AK4
A43	VSS 133	AK4
A44	VSS 134	AK4
A45	VSS 135	AK4
A46	VSS 136	AK4
A47	VSS 137	AK4
A48	VSS 138	AK4
A49	VSS 139	AK4
A50	VSS 140	AK4
A51	VSS 141	AK4
A52	VSS 142	AK4
A53	VSS 143	AK4
A54	VSS 144	AK4
A55	VSS 145	AK4
A56	VSS 146	AK4
A57	VSS 147	AK4
A58	VSS 148	AK4
A59	VSS 149	AK4
A60	VSS 150	AK4
A61	VSS 151	AK4
A62	VSS 152	AK4
A63	VSS 153	AK4
A64	VSS 154	AK4
A65	VSS 155	AK4
A66	VSS 156	AK4
A67	VSS 157	AK4
A68	VSS 158	AK4
A69	VSS 159	AK4
A70	VSS 160	AK4
A71	VSS 161	AK4
A72	VSS 162	AK4

COMETLAKE-H-CPU_B0A1440

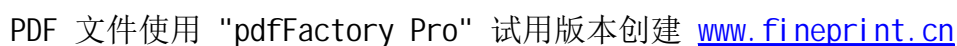
LC10		
AW5	VSS 100	B115
AW6	VSS 101	B115
AW7	VSS 102	B115
AW8	VSS 103	B115
AW9	VSS 104	B115
AW10	VSS 105	B115
AW11	VSS 106	B115
AW12	VSS 107	B115
AW13	VSS 108	B115
AW14	VSS 109	B115
AW15	VSS 110	B115
AW16	VSS 111	B115
AW17	VSS 112	B115
AW18	VSS 113	B115
AW19	VSS 114	B115
AW20	VSS 115	B115
AW21	VSS 116	B115
AW22	VSS 117	B115
AW23	VSS 118	B115
AW24	VSS 119	B115
AW25	VSS 120	B115
AW26	VSS 121	B115
AW27	VSS 122	B115
AW28	VSS 123	B115
AW29	VSS 124	B115
AW30	VSS 125	B115
AW31	VSS 126	B115
AW32	VSS 127	B115
AW33	VSS 128	B115
AW34	VSS 129	B115
AW35	VSS 130	B115
AW36	VSS 131	B115
AW37	VSS 132	B115
AW38	VSS 133	B115
AW39	VSS 134	B115
AW40	VSS 135	B115
AW41	VSS 136	B115
AW42	VSS 137	B115
AW43	VSS 138	B115
AW44	VSS 139	B115
AW45	VSS 140	B115
AW46	VSS 141	B115
AW47	VSS 142	B115
AW48	VSS 143	B115
AW49	VSS 144	B115
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AW56	VSS 151	B115
AW57	VSS 152	B115
AW58	VSS 153	B115
AW59	VSS 154	B115
AW60	VSS 155	B115
AW61	VSS 156	B115
AW62	VSS 157	B115
AW63	VSS 158	B115
AW64	VSS 159	B115
AW65	VSS 160	B115
AW66	VSS 161	B115
AW67	VSS 162	B115

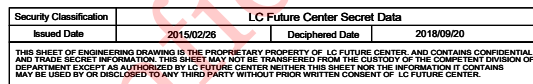
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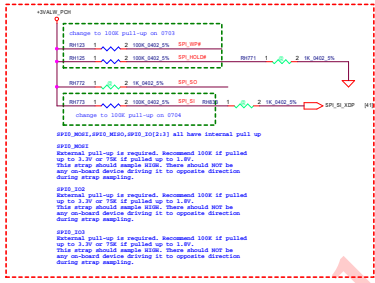
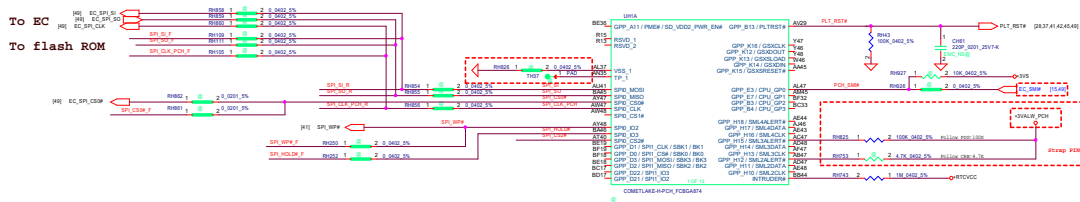
LC10		
B11	VSS 100	F15
B12	VSS 101	F15
B13	VSS 102	F15
B14	VSS 103	F15
B15	VSS 104	F15
B16	VSS 105	F15
B17	VSS 106	F15
B18	VSS 107	F15
B19	VSS 108	F15
B20	VSS 109	F15
B21	VSS 110	F15
B22	VSS 111	F15
B23	VSS 112	F15
B24	VSS 113	F15
B25	VSS 114	F15
B26	VSS 115	F15
B27	VSS 116	F15
B28	VSS 117	F15
B29	VSS 118	F15
B30	VSS 119	F15
B31	VSS 120	F15
B32	VSS 121	F15
B33	VSS 122	F15
B34	VSS 123	F15
B35	VSS 124	F15
B36	VSS 125	F15
B37	VSS 126	F15
B38	VSS 127	F15
B39	VSS 128	F15
B40	VSS 129	F15
B41	VSS 130	F15
B42	VSS 131	F15
B43	VSS 132	F15
B44	VSS 133	F15
B45	VSS 134	F15
B46	VSS 135	F15
B47	VSS 136	F15
B48	VSS 137	F15
B49	VSS 138	F15
B50	VSS 139	F15
B51	VSS 140	F15
B52	VSS 141	F15
B53	VSS 142	F15
B54	VSS 143	F15
B55	VSS 144	F15
B56	VSS 145	F15
B57	VSS 146	F15
B58	VSS 147	F15
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B62	VSS 151	F15
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B67	VSS 156	F15
B68	VSS 157	F15
B69	VSS 158	F15
B70	VSS 159	F15
B71	VSS 160	F15
B72	VSS 161	F15
B73	VSS 162	F15

COMETLAKE-H-CPU_B0A1440

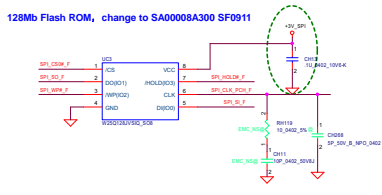
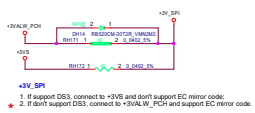
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2015/02/26		2018/09/20		COMETLAKE-H-CPU_B0A1440	
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2018-09-20				11 of 19	



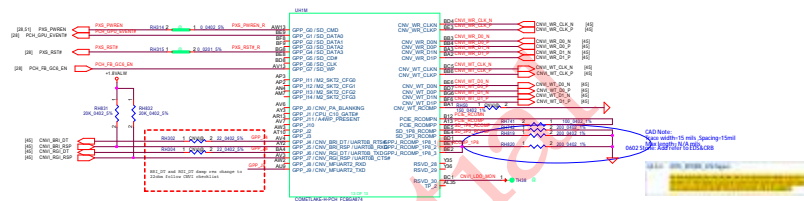
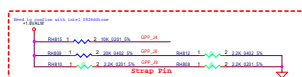
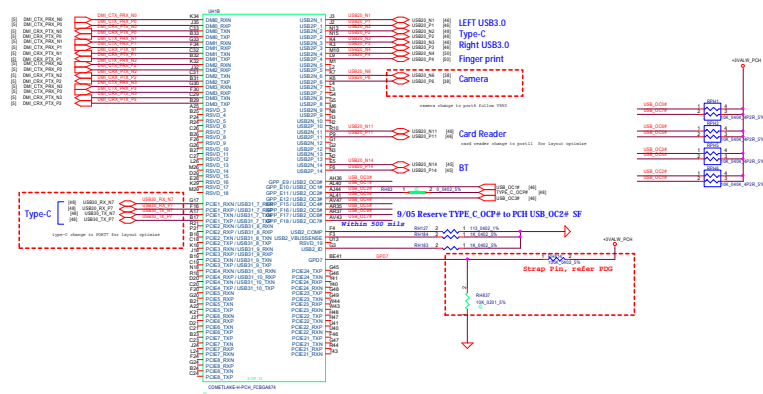




SPI_SS / SPI_MISO (Strap reserved)
 Backdoor pull-up is required. Increased SS08 if pulled up to 1.0V or 1.8V if pulled up to 1.0V.
 This strap should enable SS08. There should NOT be any on-board device driving it to opposite direction during strap sampling.
 Power Plane Primary Hall
 SPI_SS / SPI_MISO
 This signal has a weak internal pull-down.
 0. Master Attached Flash Sharing (MAFS) enabled.
 1. 1.0V Internal Flash Sharing (MAFS) enabled.
 Warning: This strap must be configured to "0" (disabled) if the SPI is not used.
 2. The internal pull-down is disabled after SS08 is disabled.
 3. The internal pull-down is disabled after SS08 is disabled.



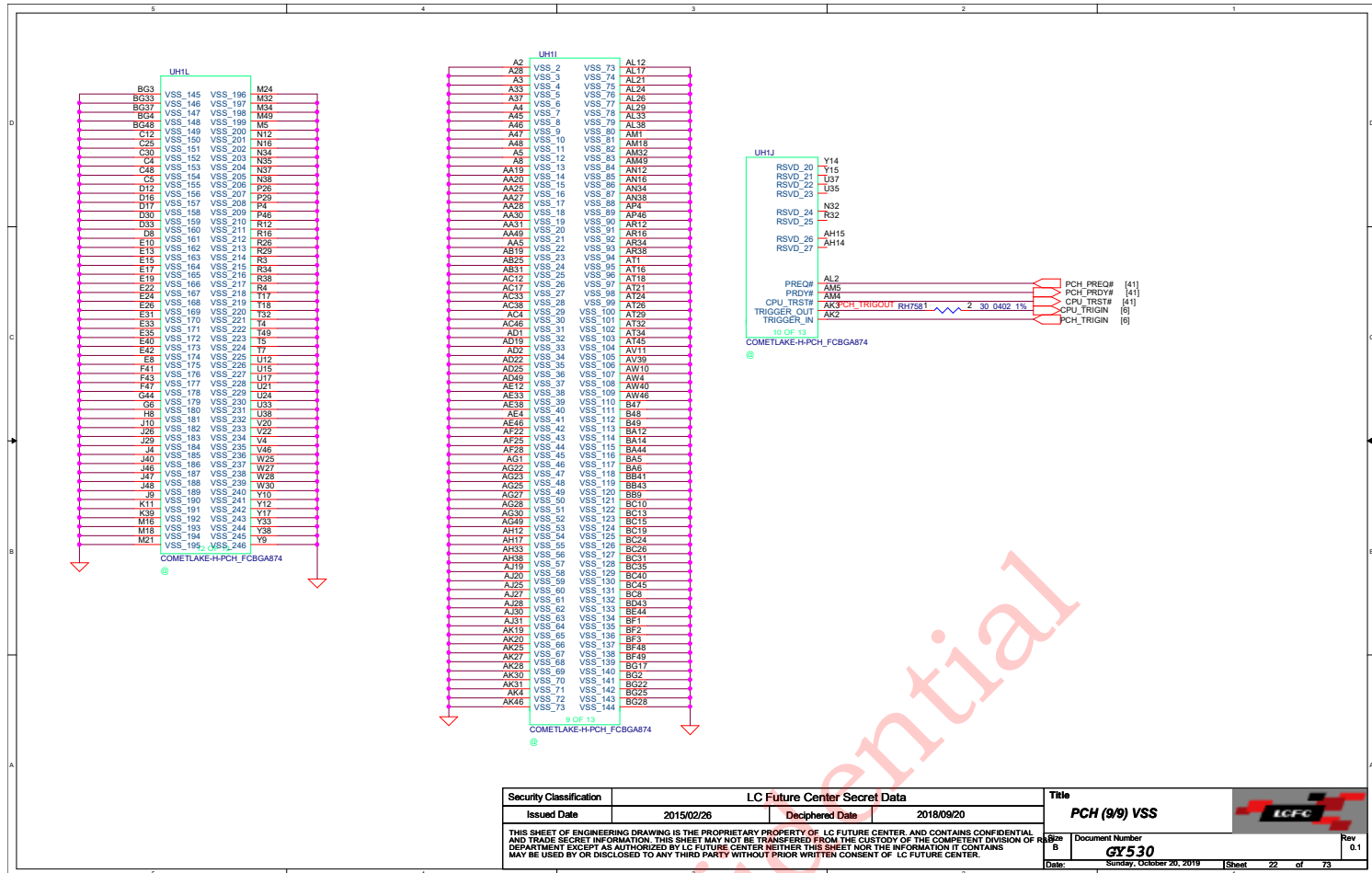
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Issued Date	2015/02/20	Declassified Date	2018/05/20
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Document Number	PCH (SPI) SP/PP/ABDEN		
Version	01		
Page	61		



Primary Well Group J (1.8 V Only)


Signal	Usage	When Activated	Comments
SPF_26 / UART_SSP_0[†] UART_SSP_1[†]	TX/RX Frequency Stable	During setup of UART0 & 1	<p>This signal is used to reset external pull-downs. An external pull-up is tied to one of the two pins (pins 30 and 31) and is not supported on the DCK.</p> <p>1 = 26 MHz (frequency of the PLL output)</p> <p>1 = 240MHz TX/RX frequency (optional)</p> <p>Notes:</p> <ol style="list-style-type: none"> 1 = external pull-down is disabled after <i>SPF0EN</i> is deasserted. 2 = pull-up is in the primary state. <p>An external pull-up or pull-down is required.</p> <p>0 = <i>SPF0EN</i> is asserted, <i>SPF0EN</i> is deasserted</p> <p>1 = <i>SPF0EN</i> is asserted, <i>SPF0EN</i> is deasserted</p> <p>This signal has a weak internal pull-down</p> <p>0 = <i>SPF0EN</i> is asserted to 1.50 V</p> <p>1 = <i>SPF0EN</i> is asserted to 1.8V</p> <p>Note: The primary state of the signal is 1.8V. Also, this signal may be used to reset the DCK.</p>
SPF_36 / UART_SSP_2[†] UART_SSP_3[†]	TX/RX Frequency Stable	During setup of UART2 & 3	<p>This signal is used to reset external pull-downs. An external pull-up is tied to one of the two pins (pins 30 and 31) and is not supported on the DCK.</p> <p>1 = 36 MHz (frequency of the PLL output)</p> <p>1 = 240MHz TX/RX frequency (optional)</p> <p>Notes:</p> <ol style="list-style-type: none"> 1 = external pull-down is disabled after <i>SPF2EN</i> is deasserted. 2 = pull-up is in the primary state. <p>An external pull-up or pull-down is required.</p> <p>0 = <i>SPF2EN</i> is asserted, <i>SPF2EN</i> is deasserted</p> <p>1 = <i>SPF2EN</i> is asserted, <i>SPF2EN</i> is deasserted</p> <p>This signal has a weak internal pull-down</p> <p>0 = <i>SPF2EN</i> is asserted to 1.50 V</p> <p>1 = <i>SPF2EN</i> is asserted to 1.8V</p> <p>Note: The primary state of the signal is 1.8V. Also, this signal may be used to reset the DCK.</p>
SPF_46 / UART_SSP_4[†] UART_SSP_5[†]	TX/RX Frequency Stable	During setup of UART4 & 5	<p>This signal is used to reset external pull-downs. An external pull-up is tied to one of the two pins (pins 30 and 31) and is not supported on the DCK.</p> <p>1 = 46 MHz (frequency of the PLL output)</p> <p>1 = 240MHz TX/RX frequency (optional)</p> <p>Notes:</p> <ol style="list-style-type: none"> 1 = external pull-down is disabled after <i>SPF4EN</i> is deasserted. 2 = pull-up is in the primary state. <p>An external pull-up or pull-down is required.</p> <p>0 = <i>SPF4EN</i> is asserted, <i>SPF4EN</i> is deasserted</p> <p>1 = <i>SPF4EN</i> is asserted, <i>SPF4EN</i> is deasserted</p> <p>This signal has a weak internal pull-down</p> <p>0 = <i>SPF4EN</i> is asserted to 1.50 V</p> <p>1 = <i>SPF4EN</i> is asserted to 1.8V</p> <p>Note: The primary state of the signal is 1.8V. Also, this signal may be used to reset the DCK.</p>

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			Document Number	QY530
			Scale	1:1
			Sheet	25 of 35

N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input (10K pull High)	
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	0000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

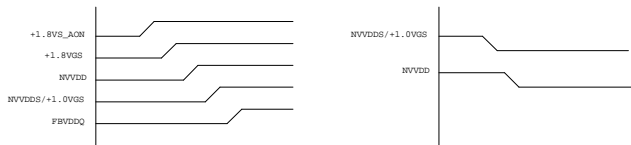
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE
SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

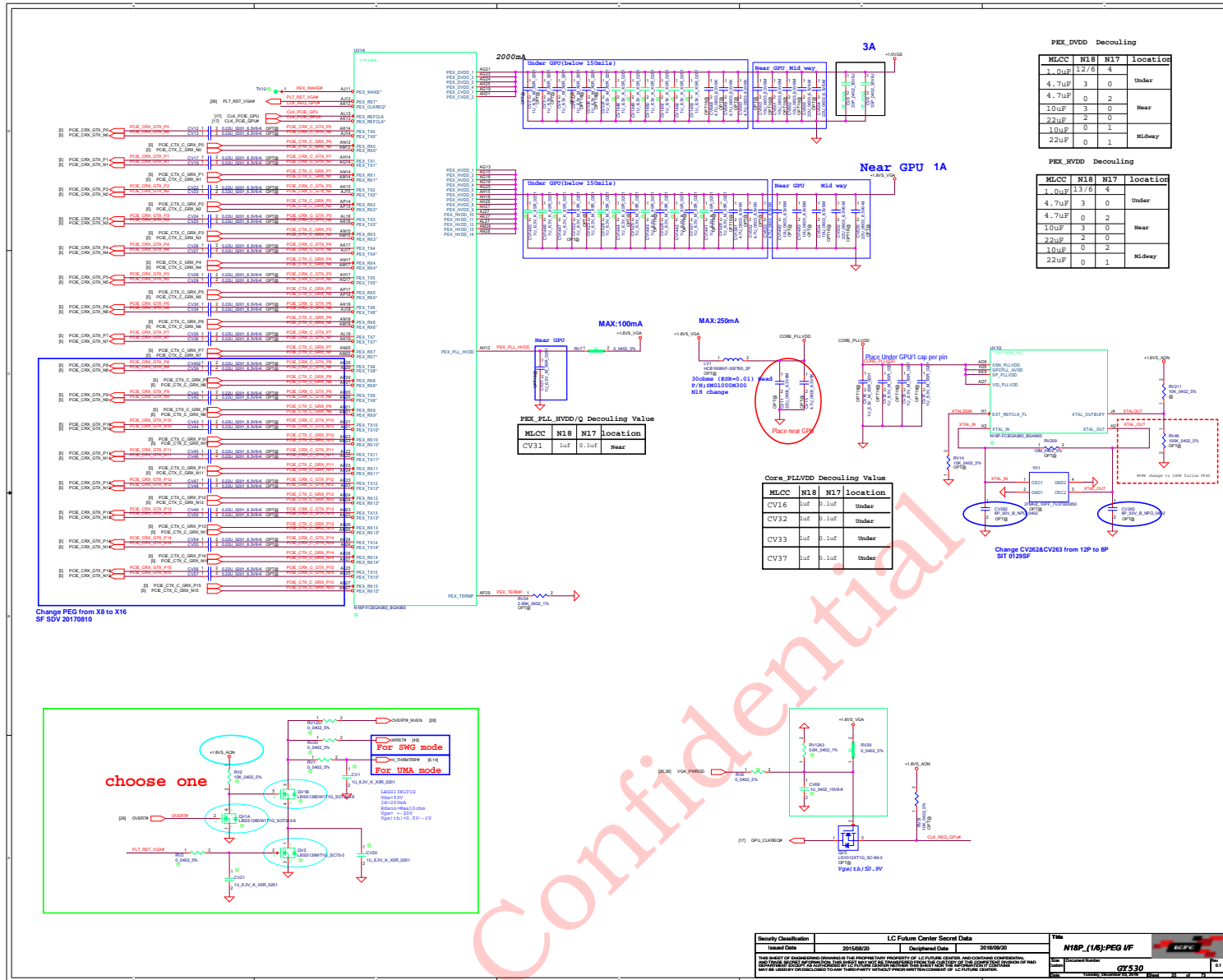
N17P-G1 Power Sequence



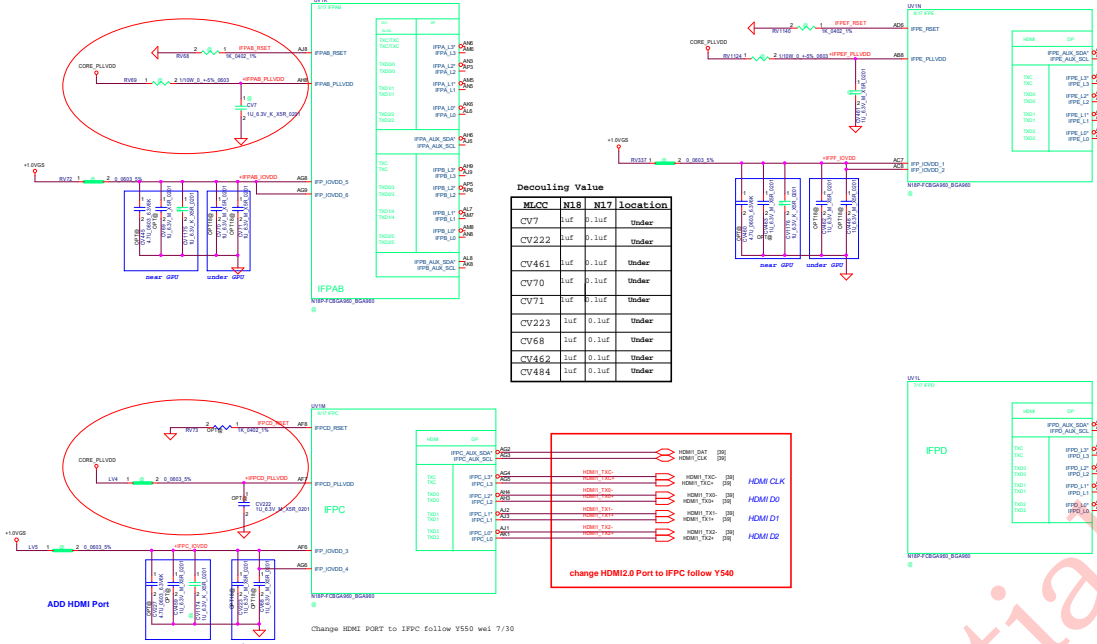
1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.
2. If from 1V8_AON to 1V8_AON/NVVDD_Pgood must NOT exceed 4ms.
3. All 1.1V devices that connect to the GPU must be powered after 1V8_AON. GPU can NOT have any 1.1V leakage path before 1V8_AON present.
4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.

1. NVVDD/1V8_AON must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.
2. All 1.1V devices that connect to the GPU must be ramp down before 1V8_AON. GPU can NOT have any 1.1V leakage path after 1V8_AON and 1.0V8_AON power down.
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

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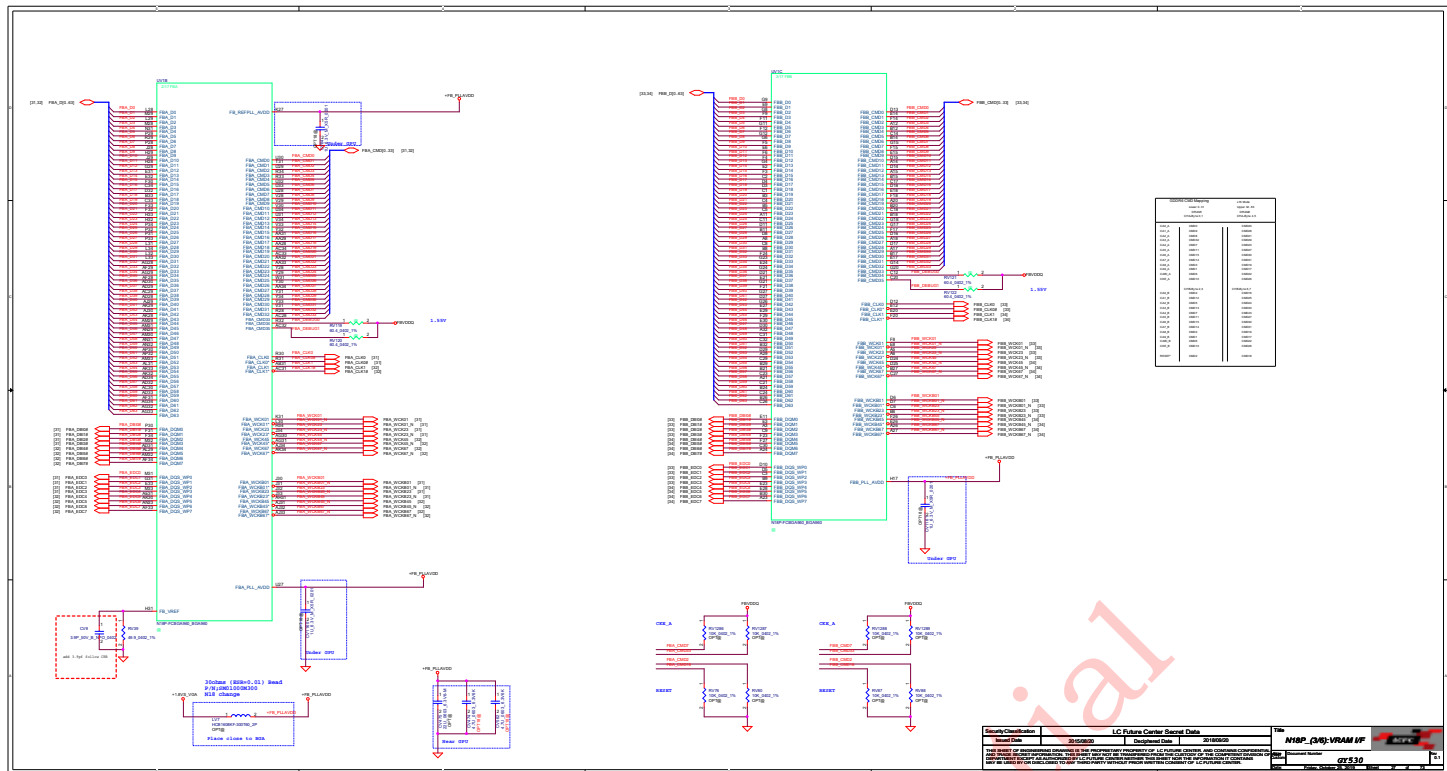
Ref NV DG-08780-001
 If an IFP link is unused, in general it should be left unconnected.
 This includes Main and Aux links.
 IFPxy_RST and IFPxy_PLLVDD (xy=AB,CD,EF)
 can be left unconnected if neither of IFPx /IFPy is in use

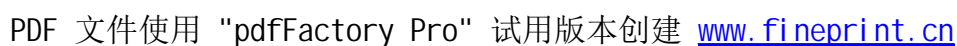


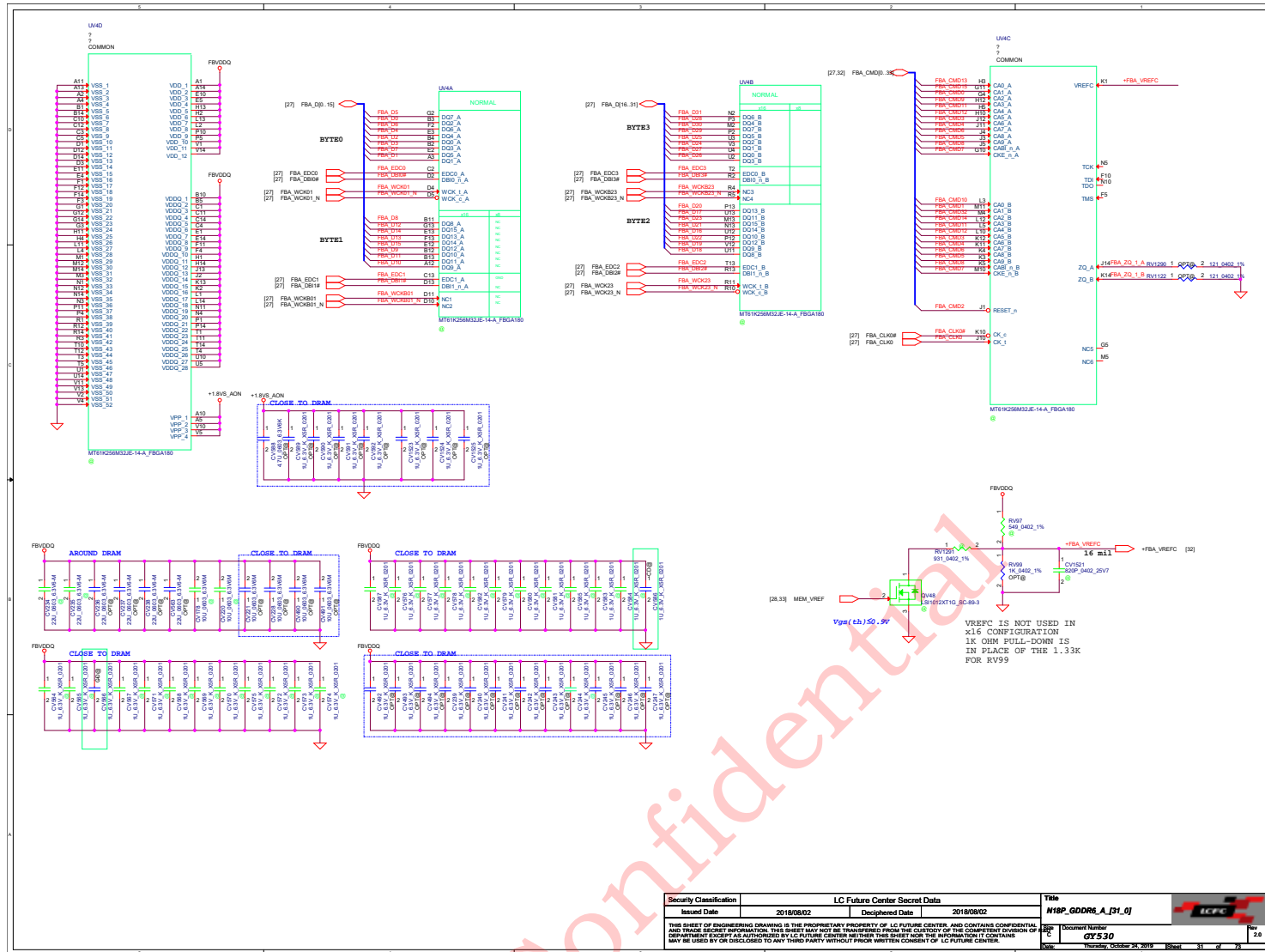
change HDMI Port to IFPC follow Y540

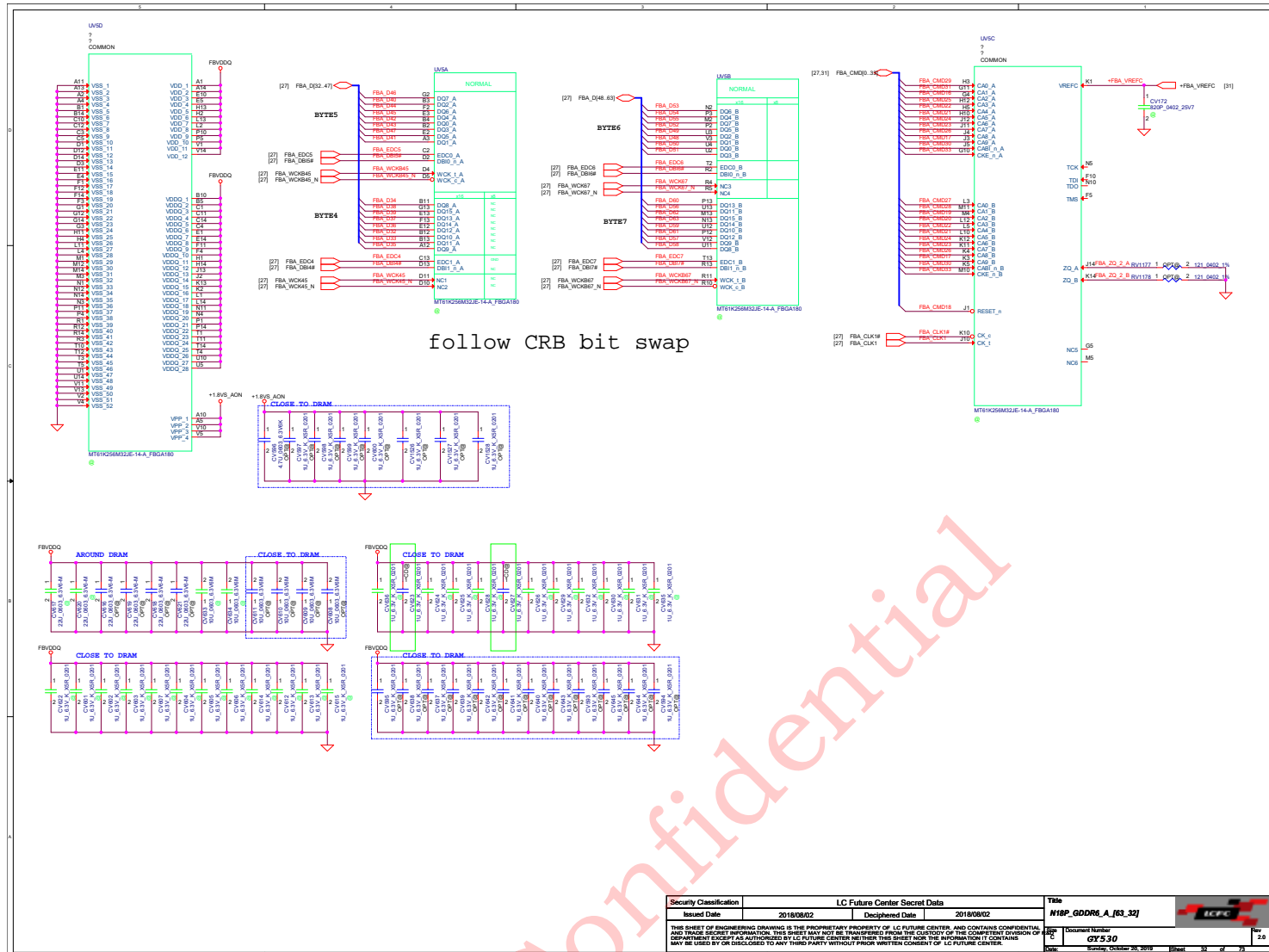
Change HDMI PORT to IFPC follow Y550 w/ 7/30

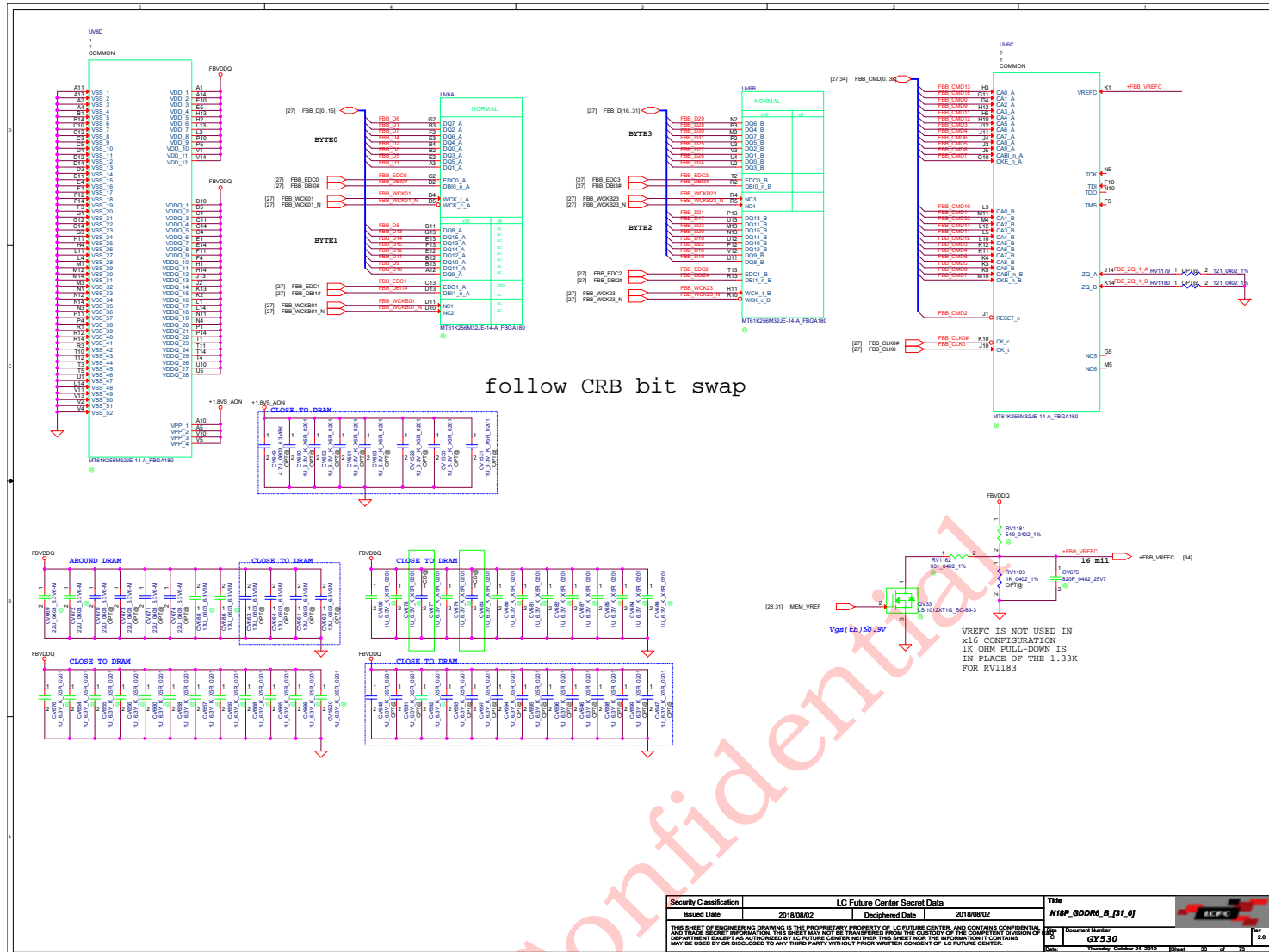
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				Page	1

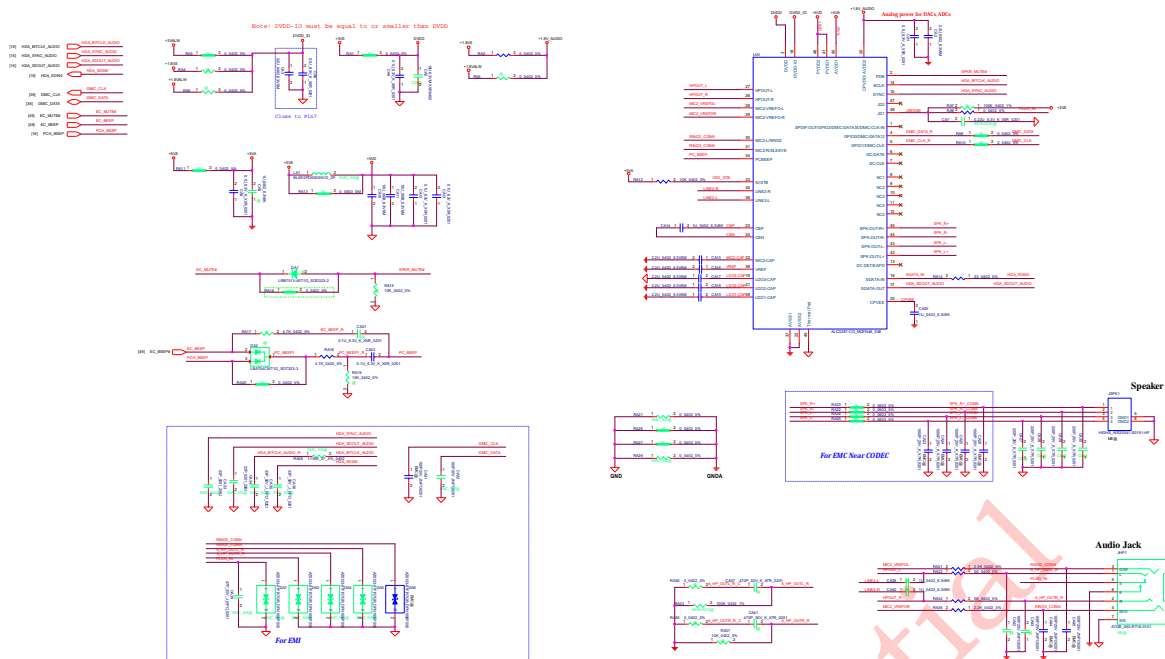






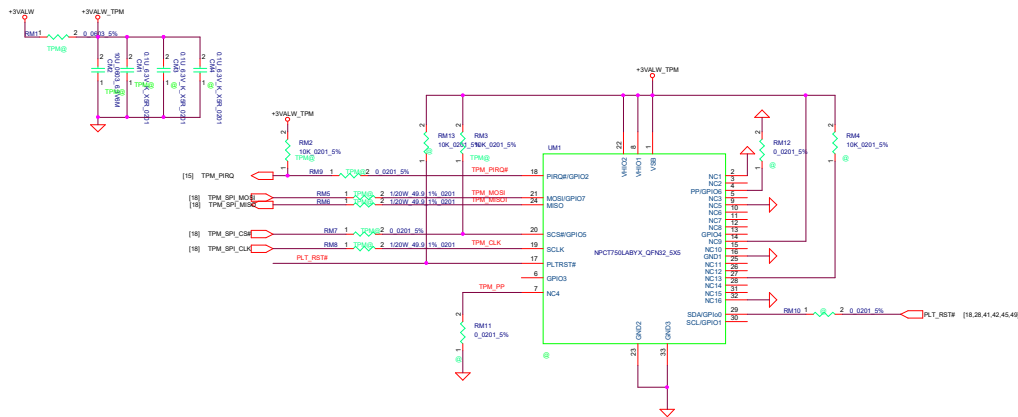




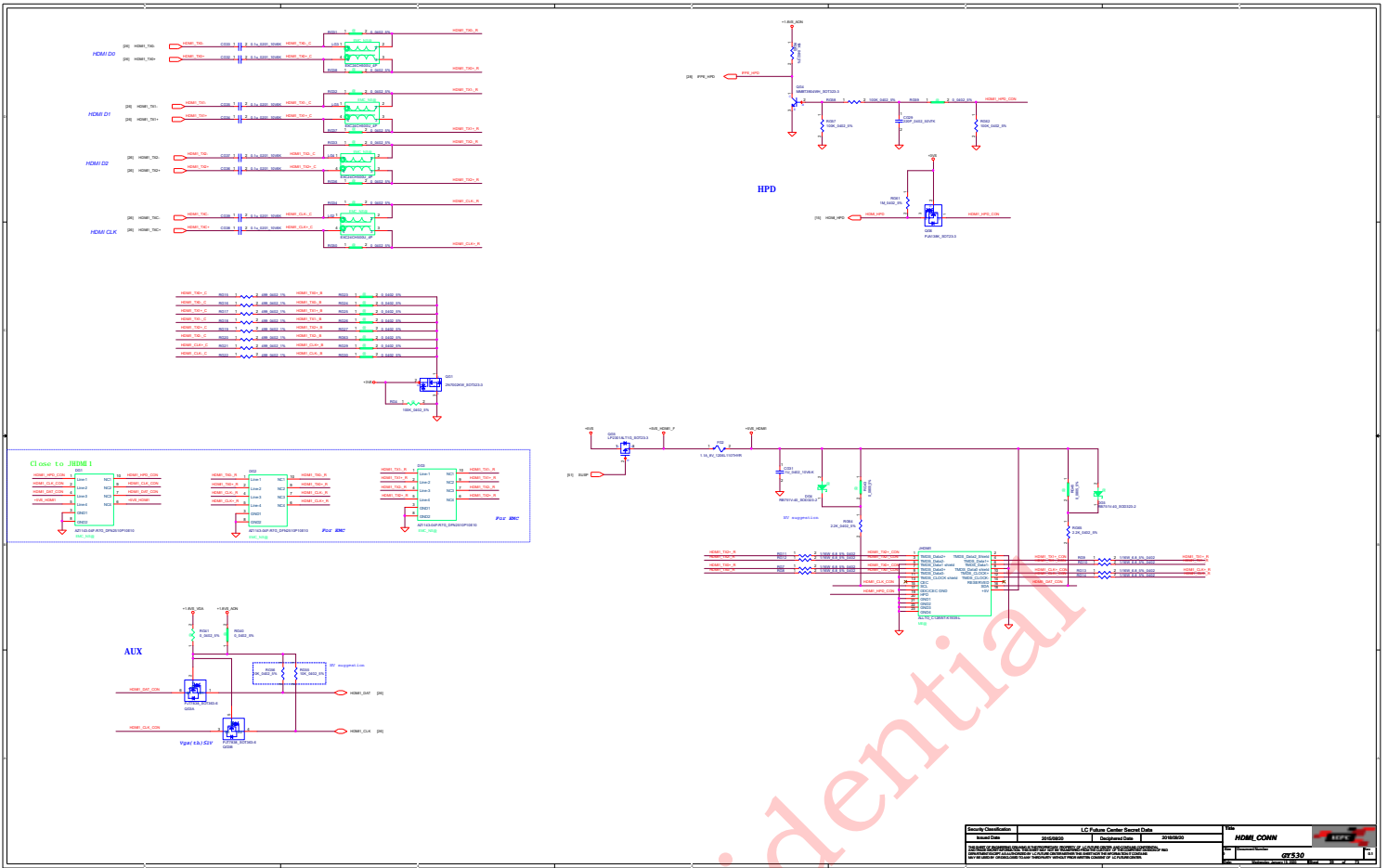


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				Date	Sunday, October 20, 2019
				Sheet	35 of 73
				Rev	0.1



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				Date	Sunday, October 25, 2015
				Sheet	40 of 78

TABLE : CPU ITP DEBUG REPORT

TABLE 1: CPU ITP DEBUG REPORT			
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R537	NO ASM	ASM	NO ASM
R9007	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
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R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

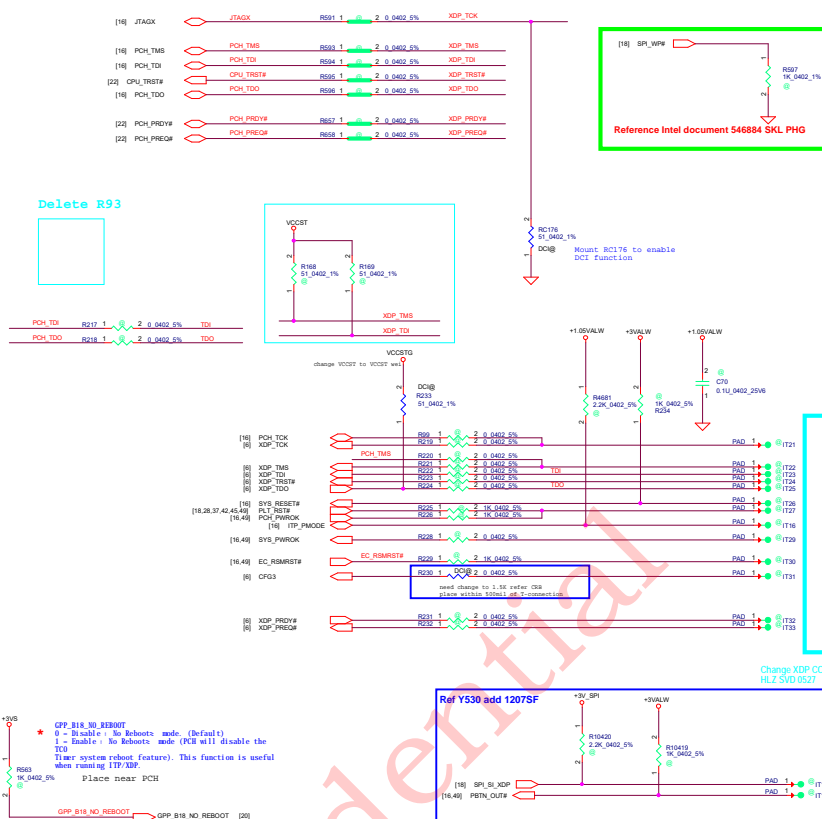
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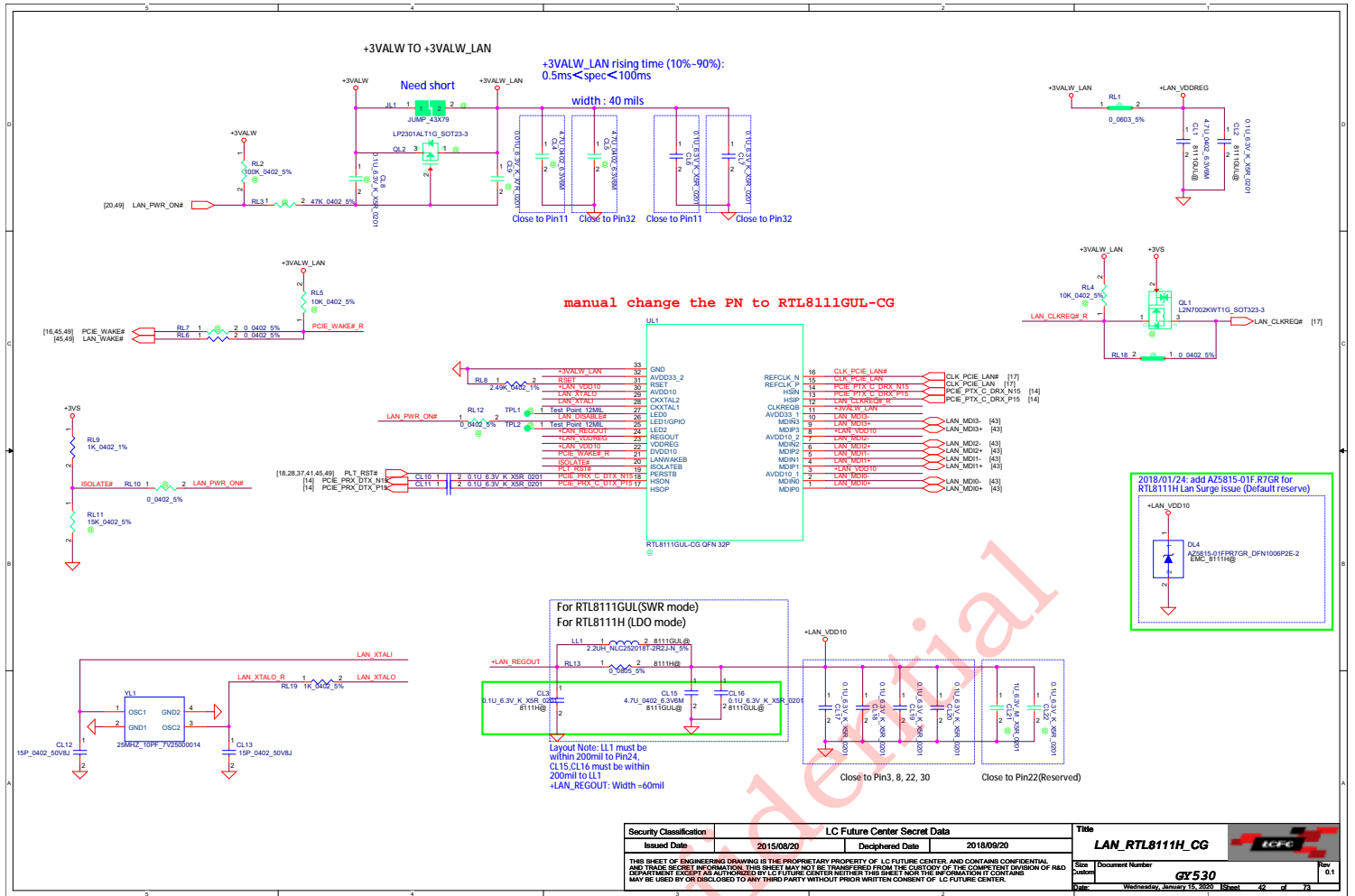
TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

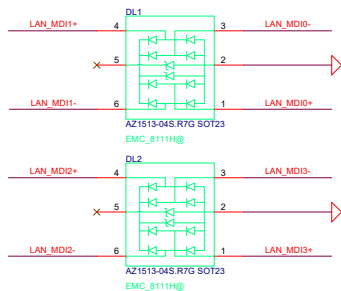
TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM



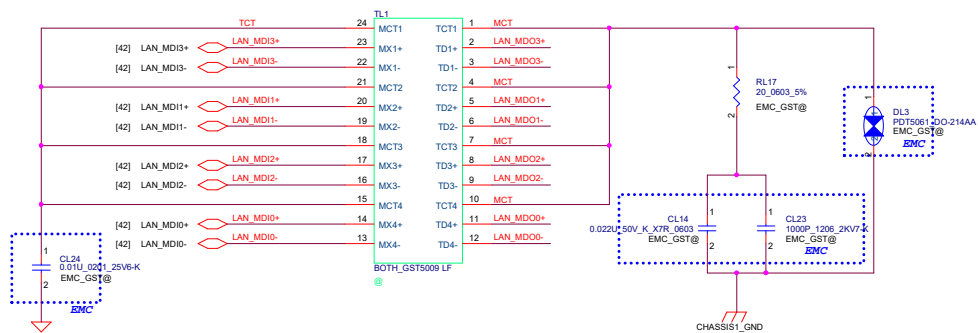
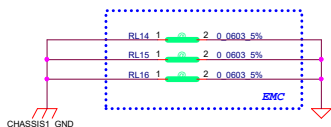


Default DL1/DL2 use
S DIO(BR) AZ1513-04S.R7G SOT23-6L
for 8111H, L340 project

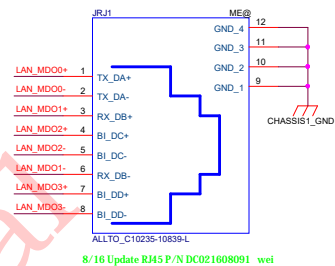
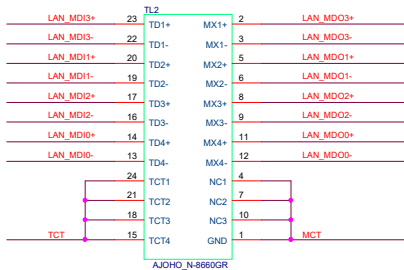


Place Close to TL1 EMC

Place Close to TL1 EMC



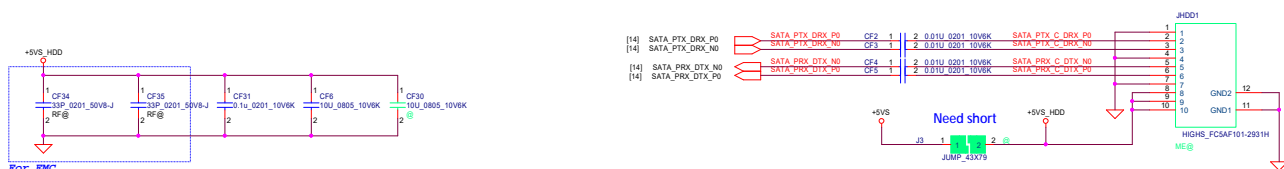
只有 8111H 可使用, 8111GUL 不可用



8/16 Update RH45 P/N DC021608091 wei

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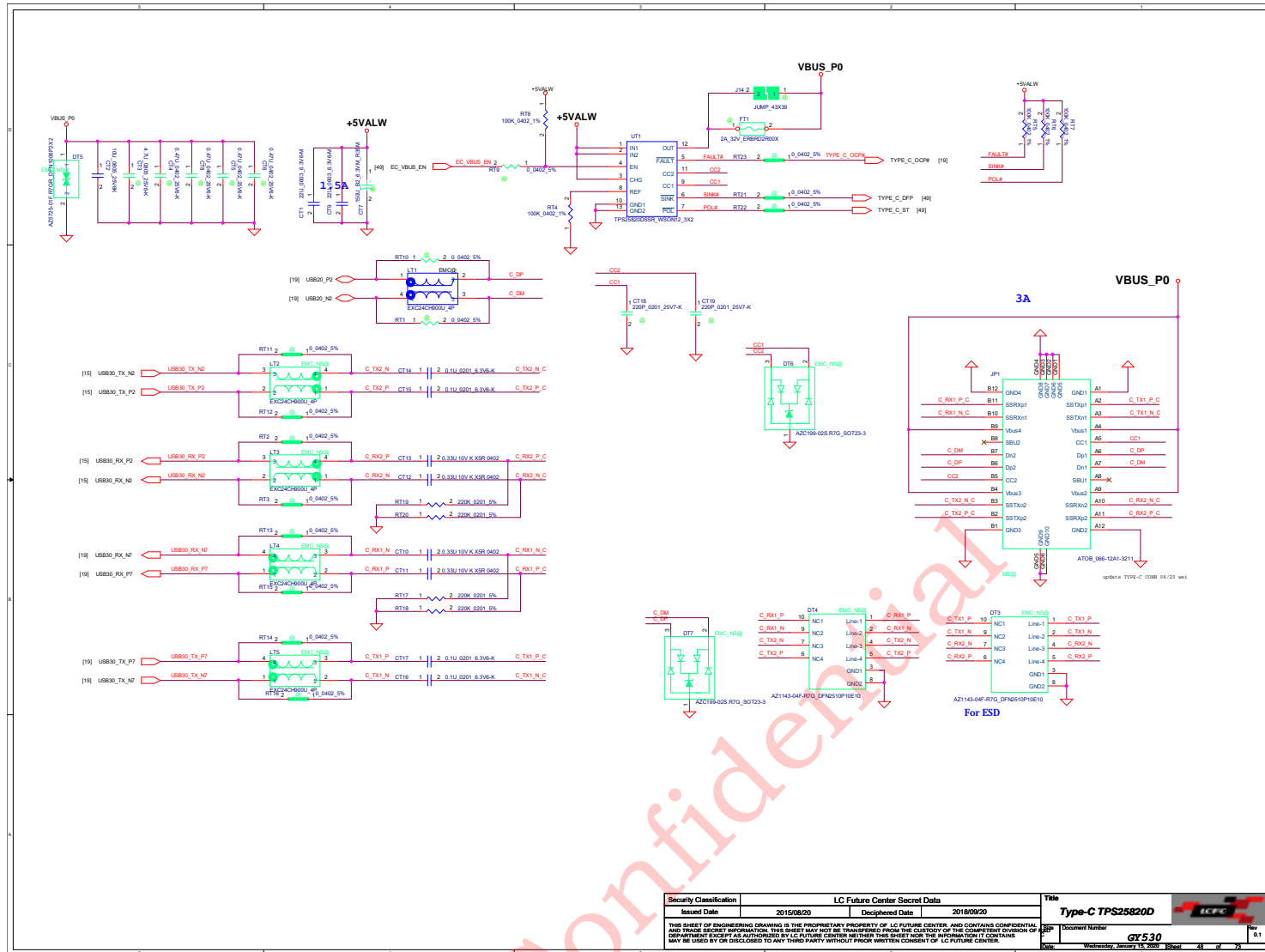
SATA HDD Conn.

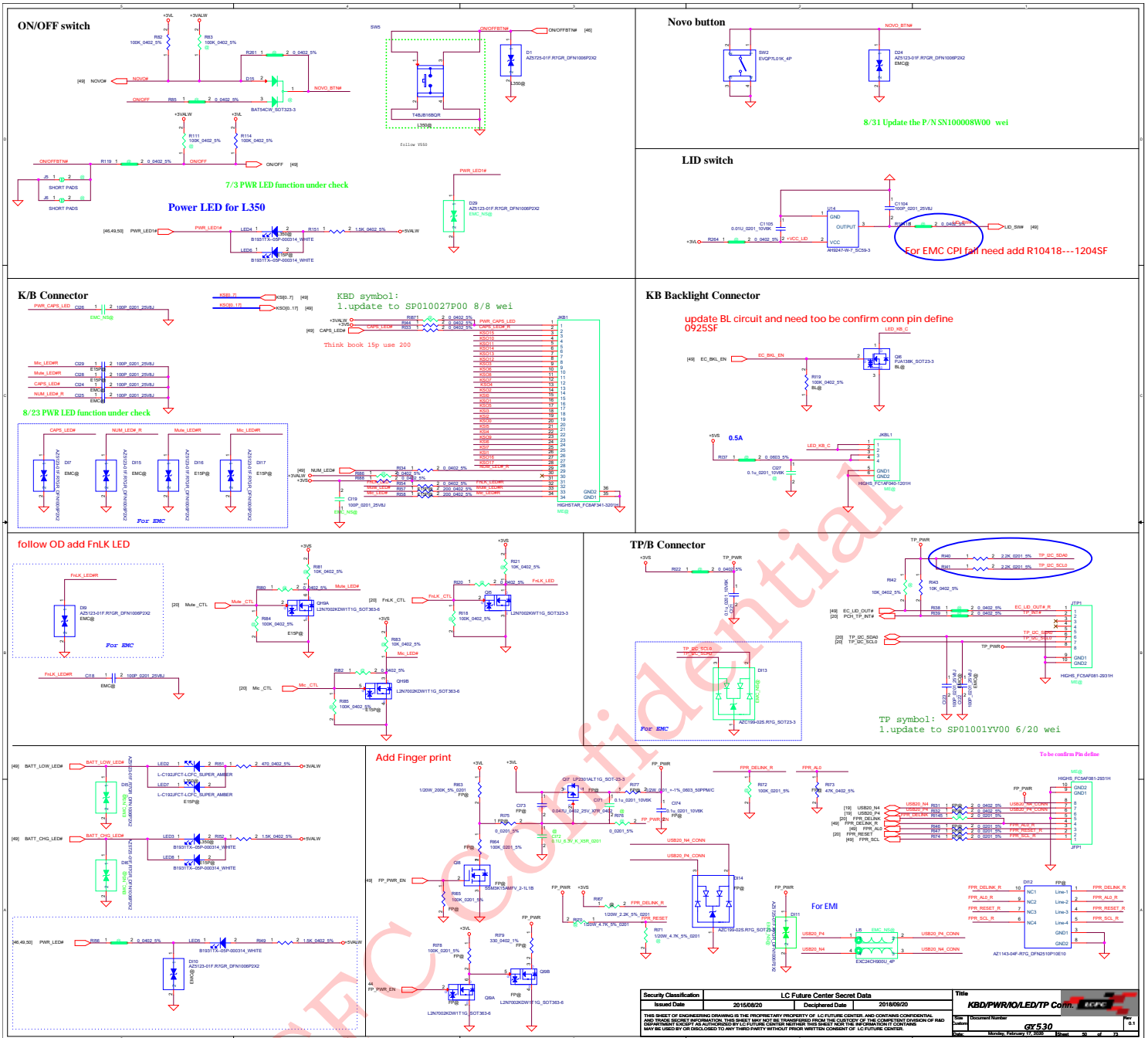


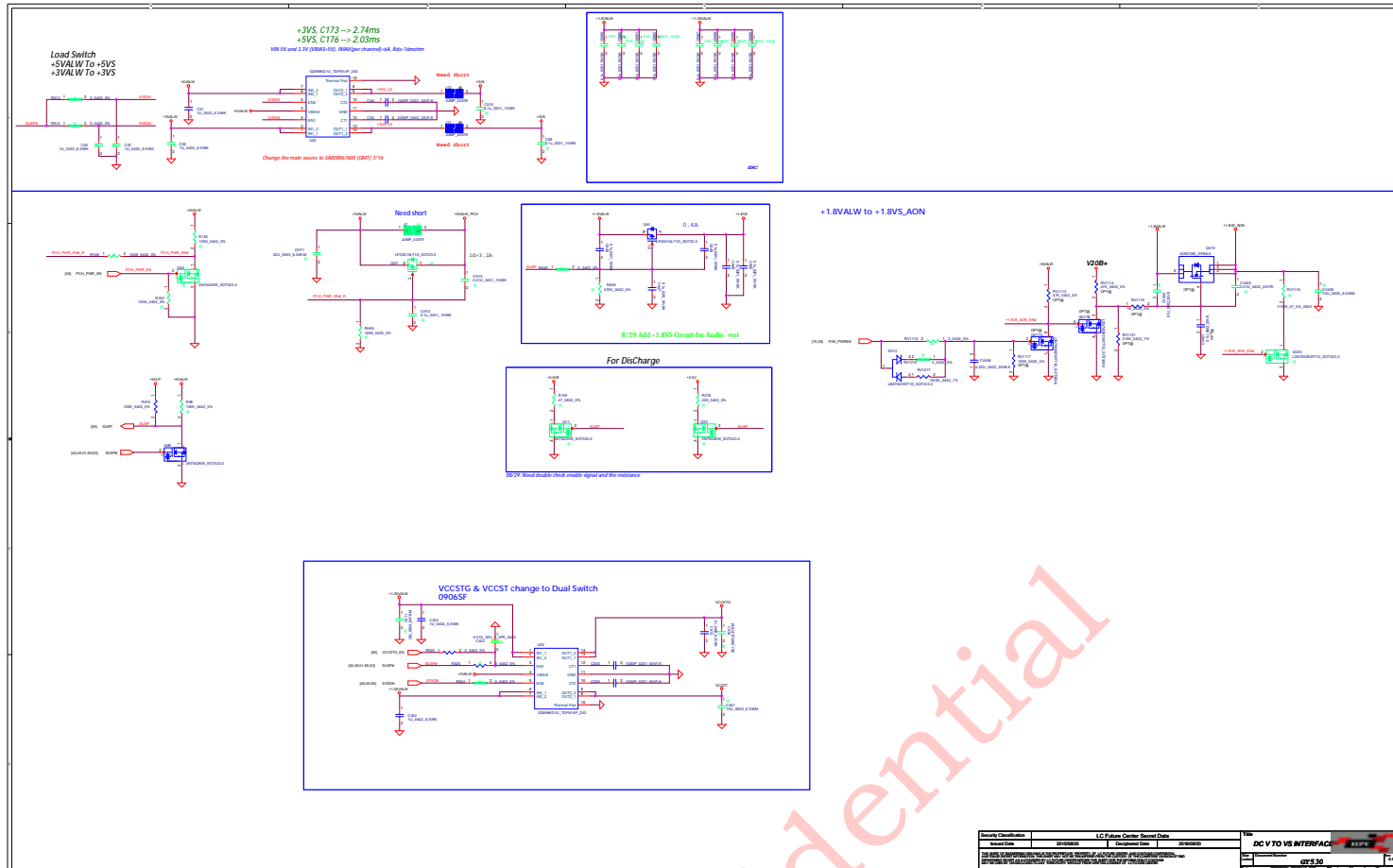
Delete SATA ODD

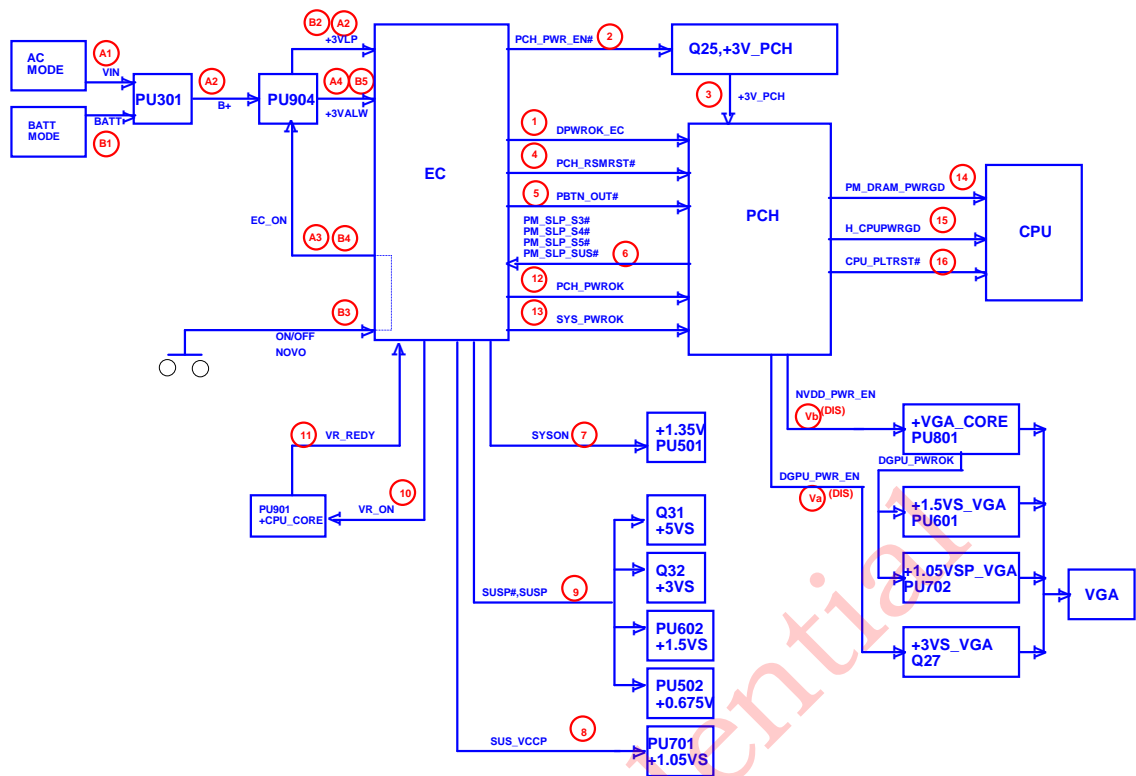
8/14 Update SF

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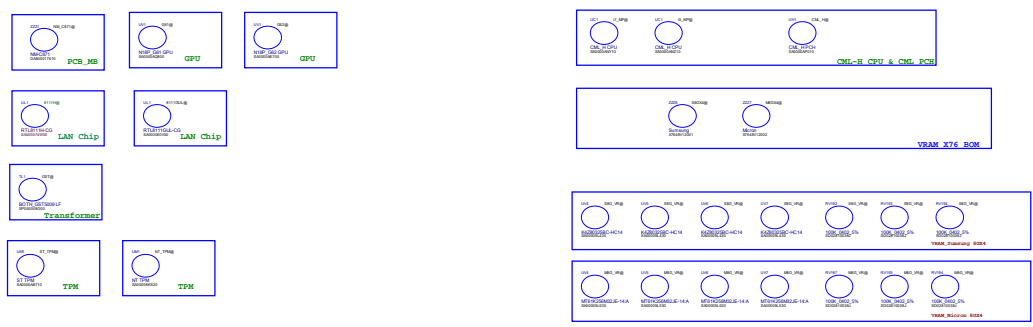




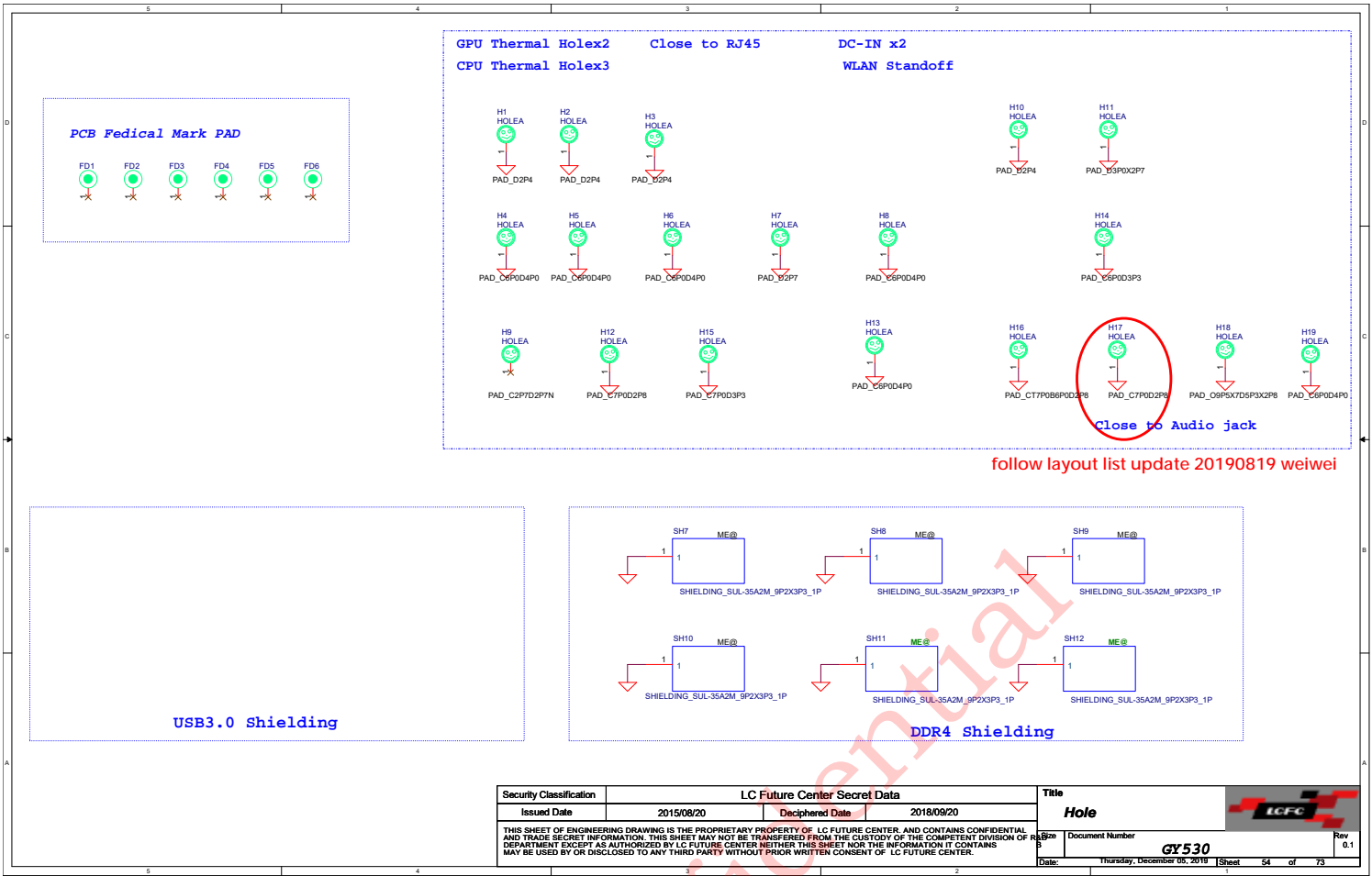




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				Date	Sunday, October 26, 2019
				Sheet	52 of 75

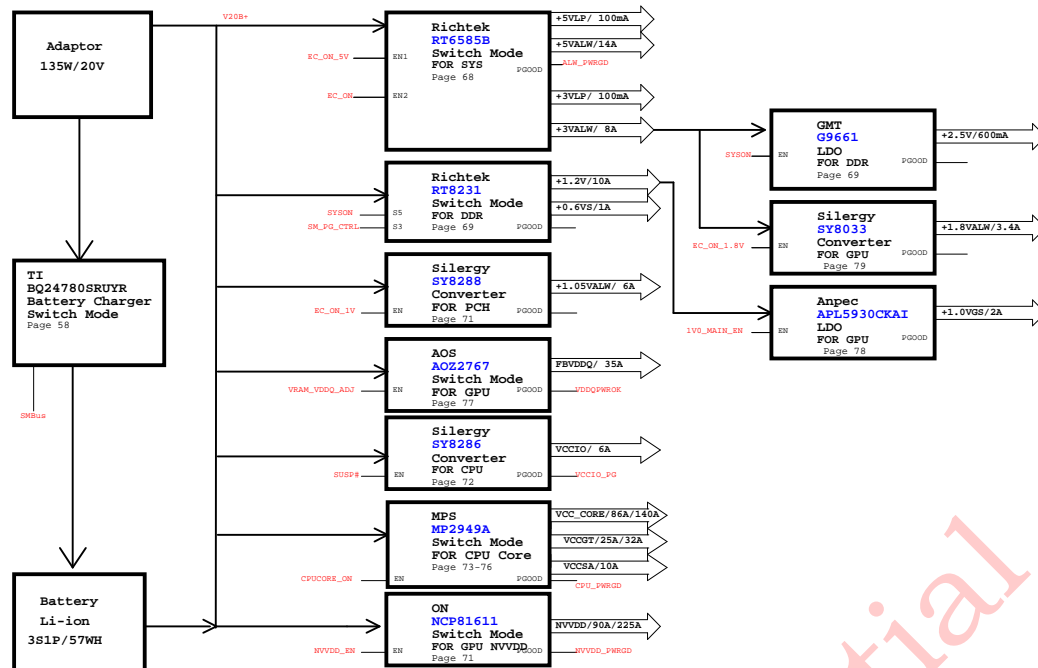


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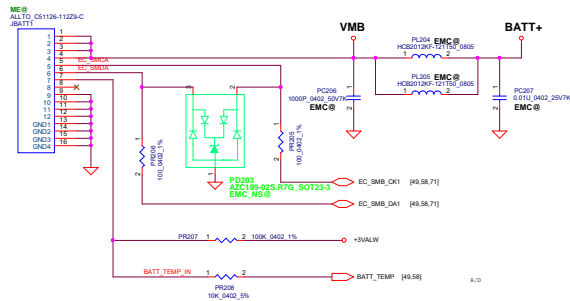
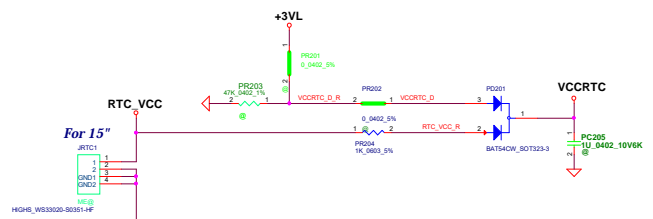
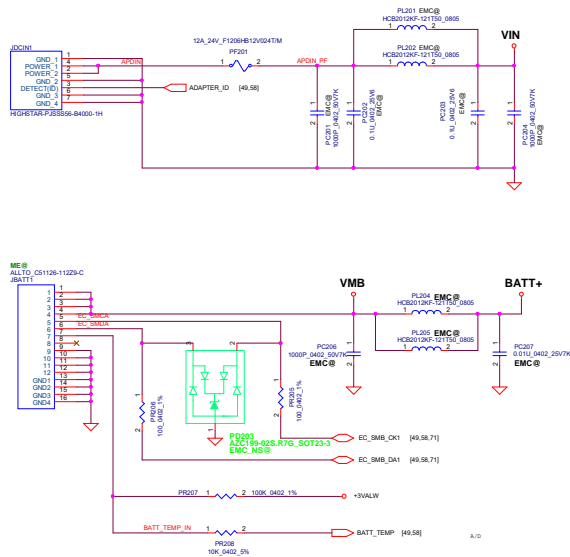


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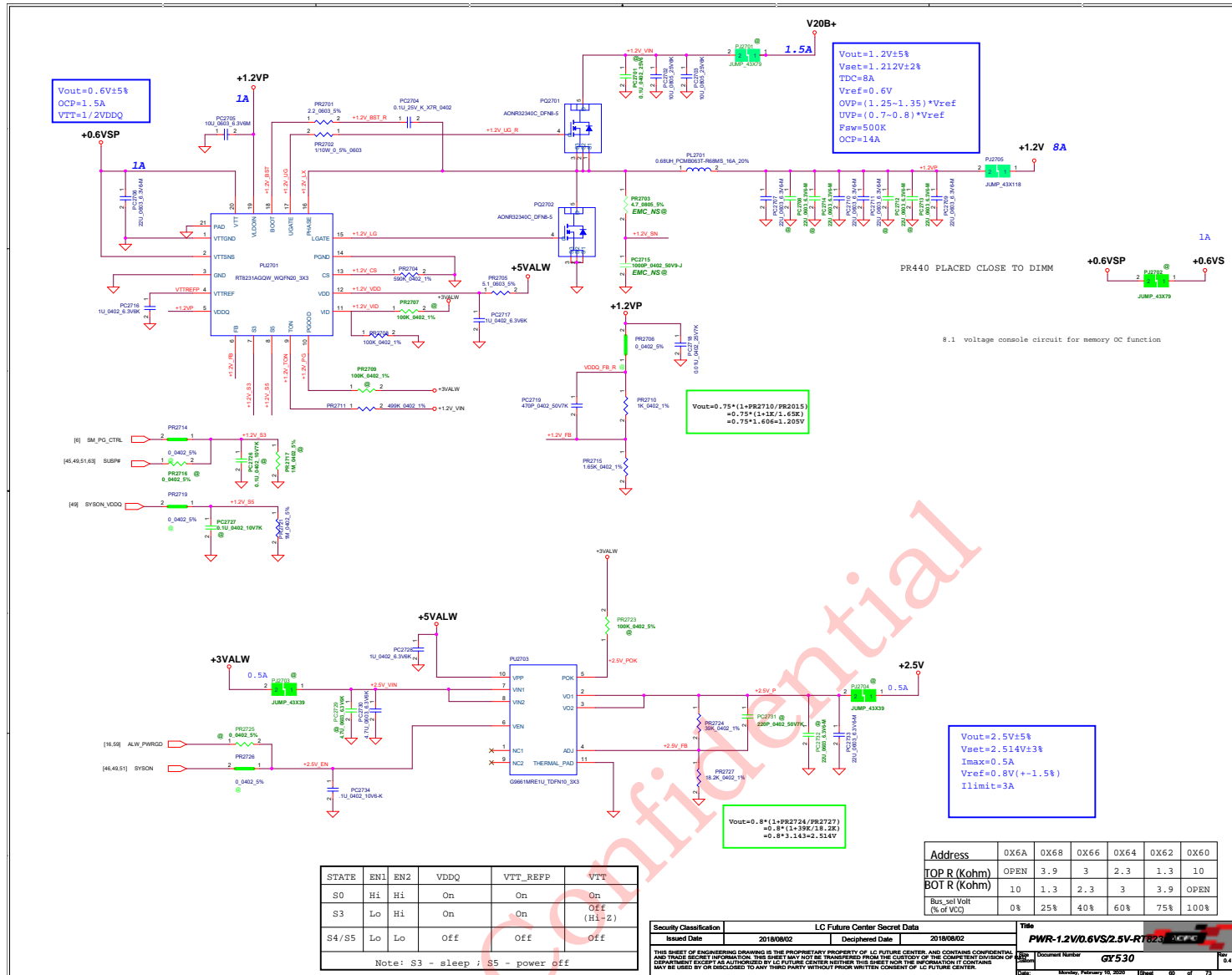
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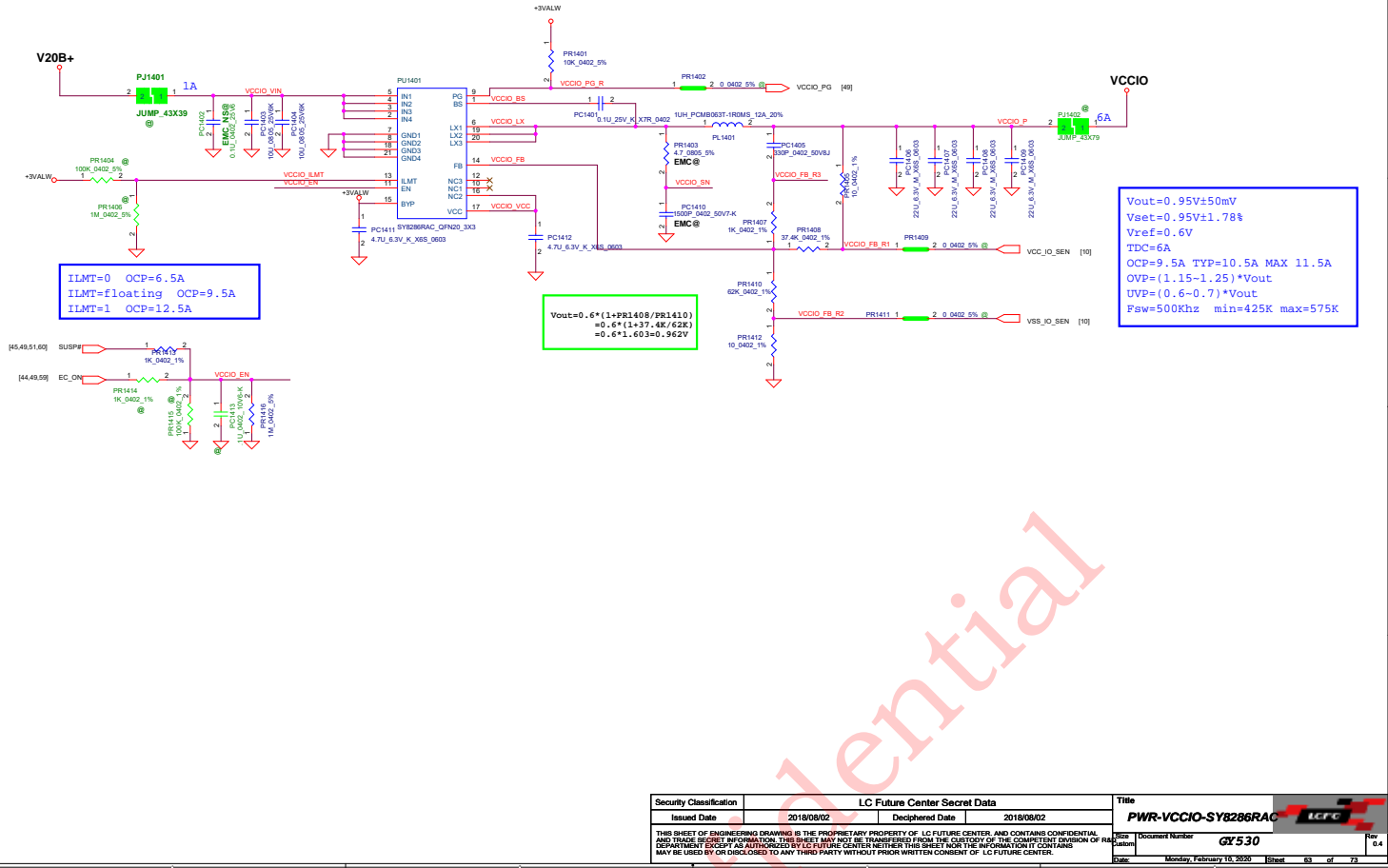


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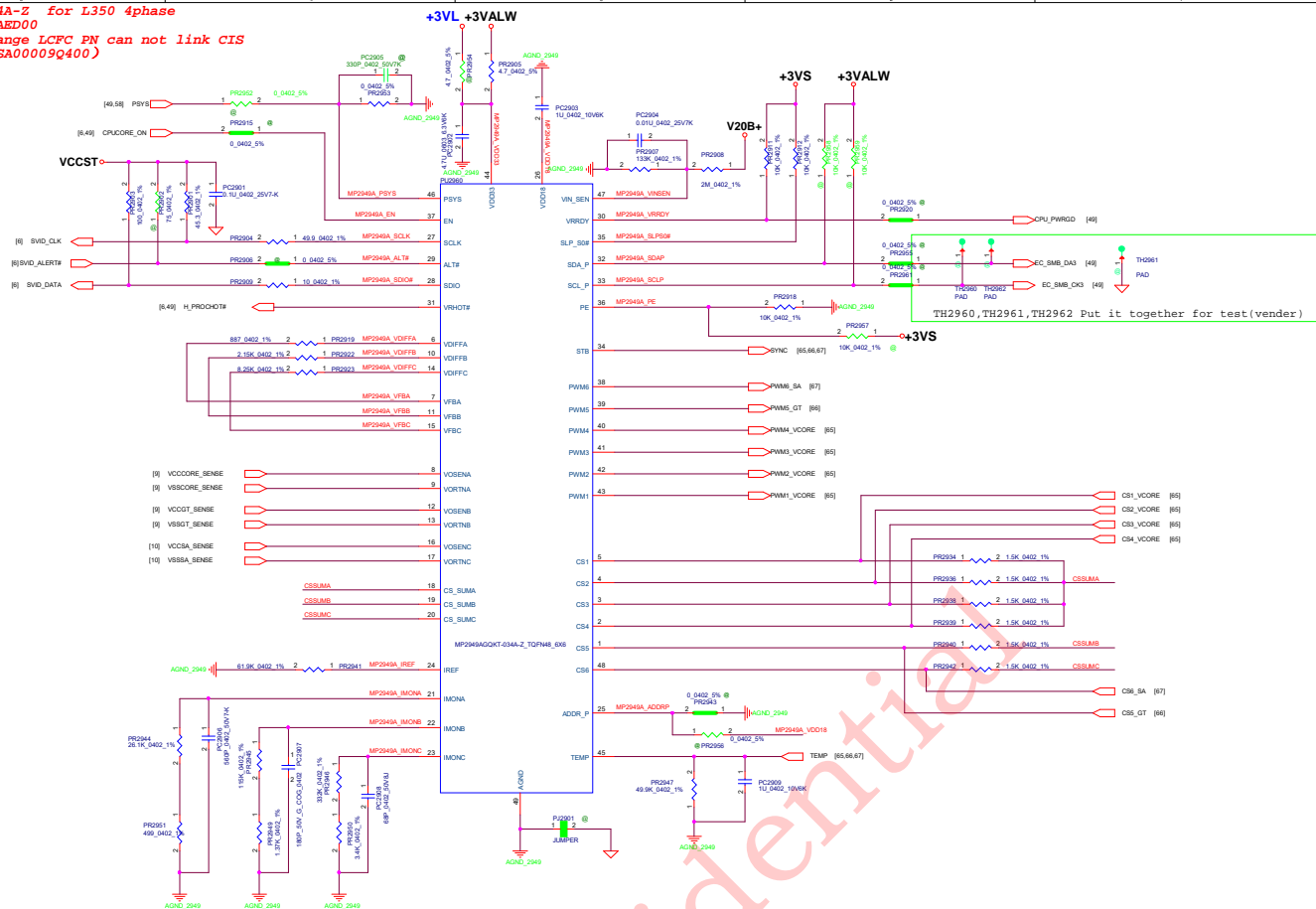


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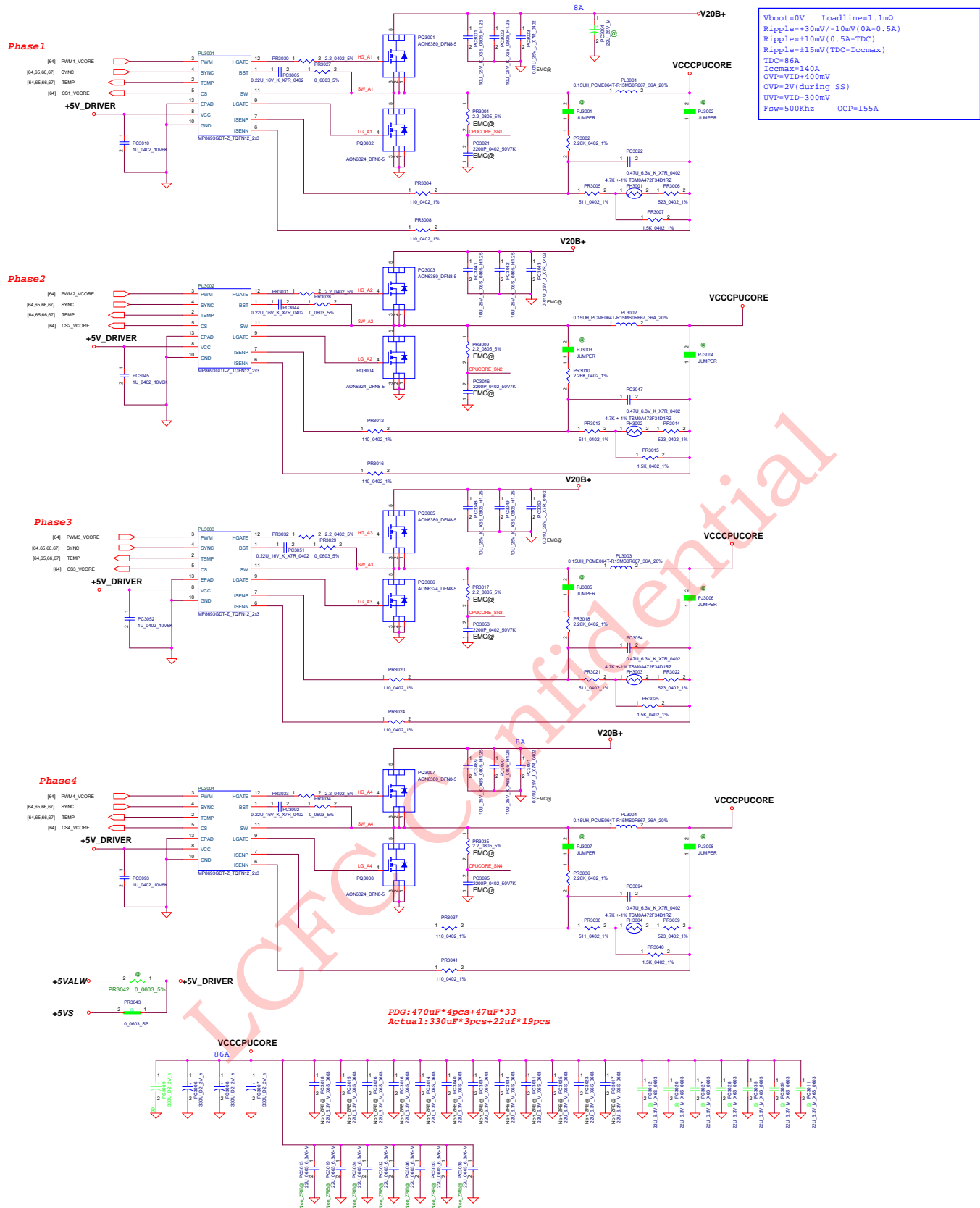
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GV530			04	
<small>Date: Version: Project No: 2000 Sheet: 01 of 05</small>				



MP2949AGQKT-034A-Z for L350 4phase
 LCFC PN:SA0000AED00
 PU2960 only change LCFC PN can not link CIS
 (L340 H82 PN:SA00009Q400)

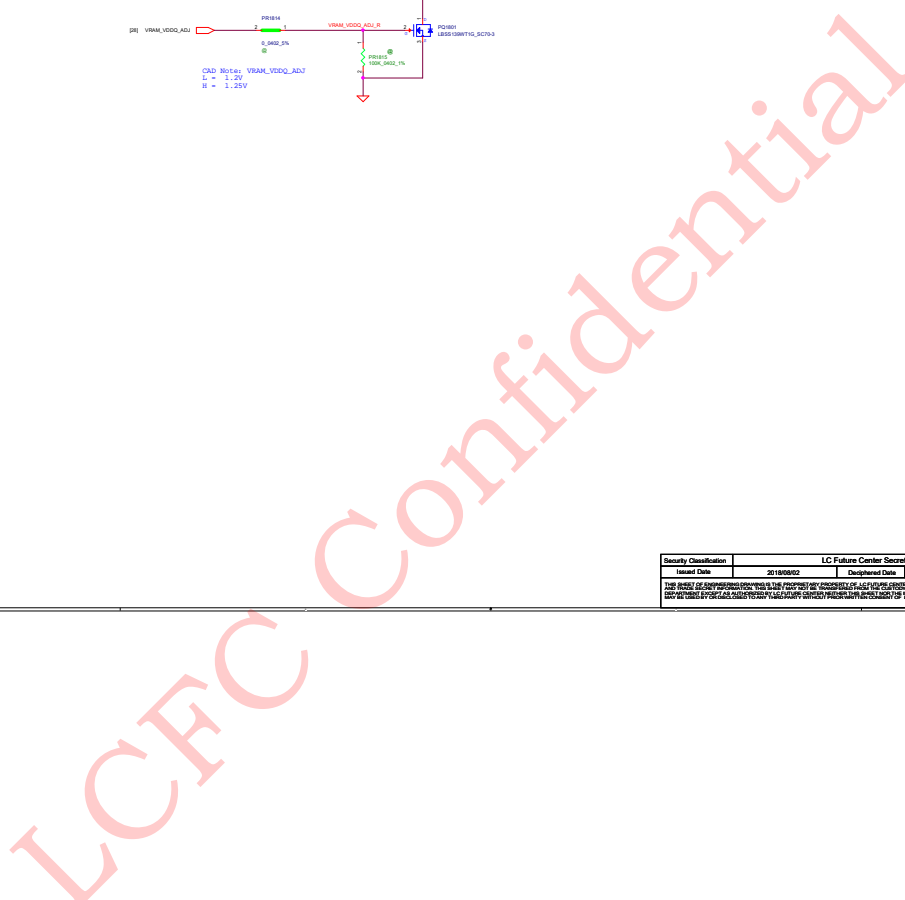


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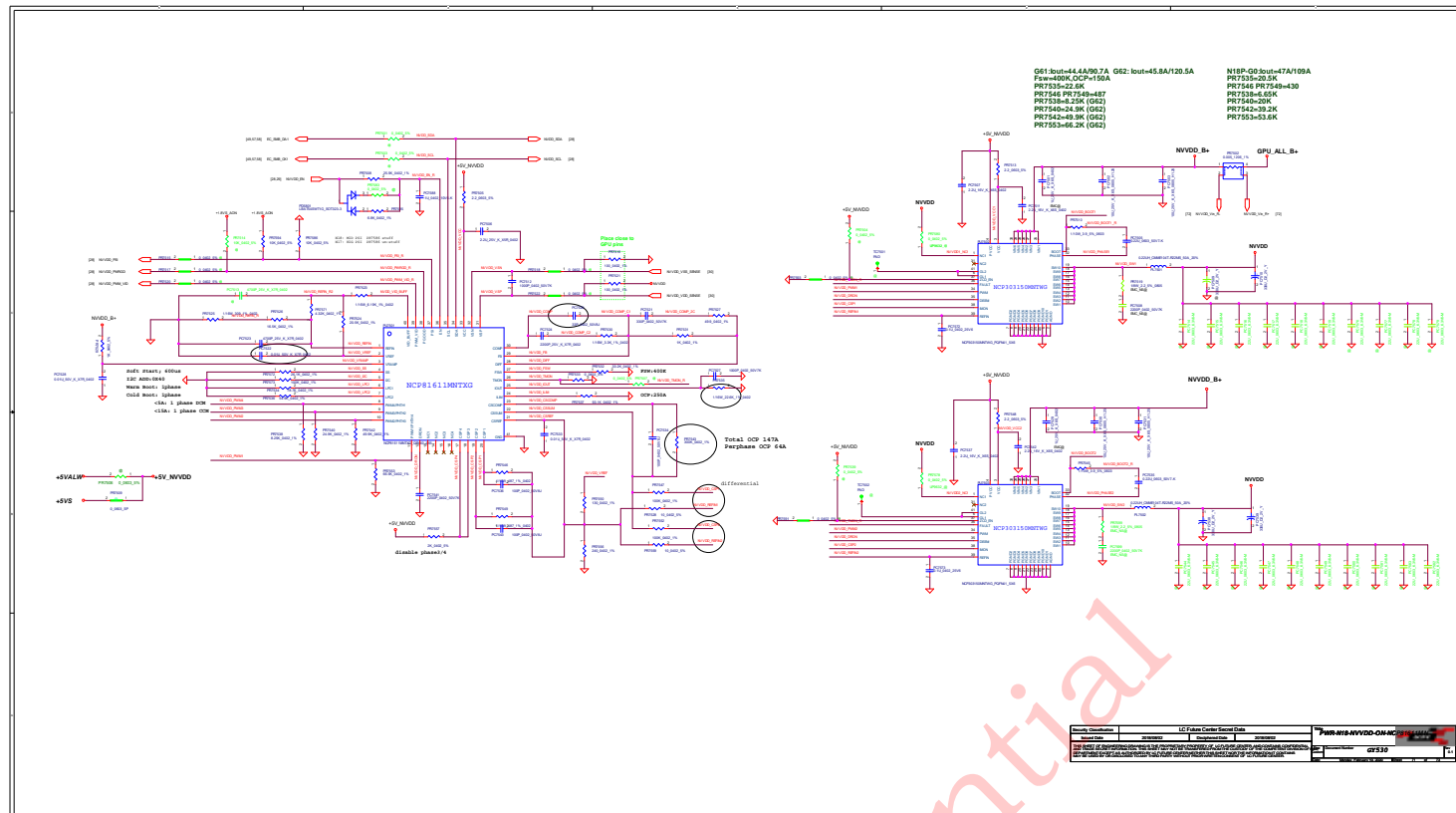


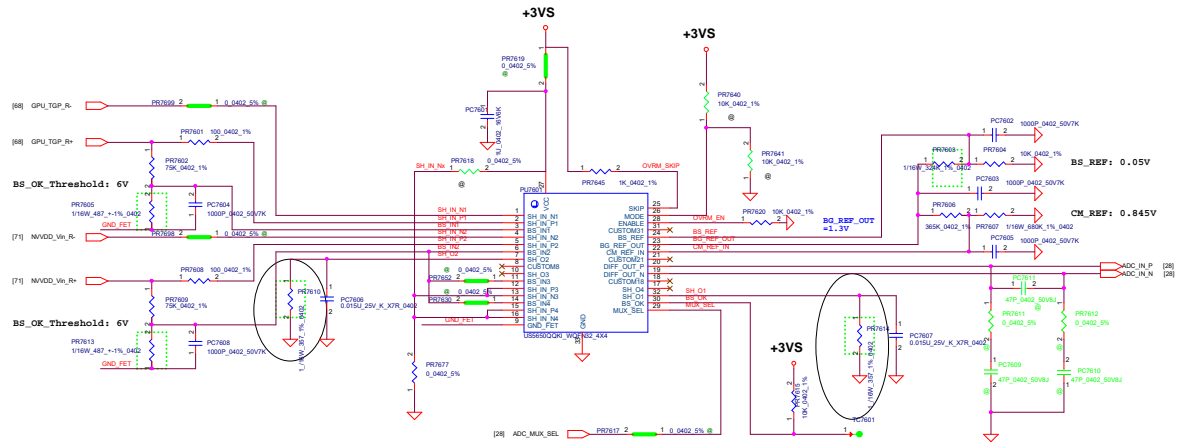
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 Ripple=±10mV(0.5A-TDC)
 Ripple=±15mV(TDC-Iccmax)
 TDC=86A
 Iccmax=140A
 OVP=VID+40mV
 OVP=2VID(during SS)
 UVP=VID-300mV
 Fsw=500Khz OCP=155A

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 PR7613=487
 PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
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 PR7602=75K
 PR7609=75K
 PC7604=1nF
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